Winning the EUV Mask Challenge

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Abstract

EUV is considered the most likely technology following the current 193nm immersion lithography. While much progress has been made during the past few years, especially since the end of 2007, still many open questions exist for the readiness of the EUV infrastructure. Listed as problem number two during the last EUV Symposium, defect free masks are still seen as a major challenge. This topic has to be addressed with enough learning cycles before enough trust in this technology is built such that the technology is ready for pilot production around 2010 and for production after 2012.

This paper will show the status of mask making processes from a perspective of a mask maker starting from the availability of mask blanks. Some of the problems and possible solutions along the mask manufacturing process up to the performance of patterned mask during exposure will be discussed. A special focus will be put on blank and mask defectivity but also some other challenges e.g. concerning blank and mask flatness and mask performance parameters will be addressed.

Introduction

With the transition from 193nm immersion lithography to EUV, major parts of the mask making and lithography infrastructure will have to change. Connected to the change in wavelength from 193nm to 13.5nm the optics in the lithography tools have to be changed from transparent lenses to mirrors in a vacuum system and likewise the mask material undergoes a similar change. EUV mask blanks are composed of an extremely flat zero-expansion material covered with a multi-layer mirror and the pattern carrying absorber material, while the backside is covered with a layer that allows electrostatic chucking to the mask holder in the exposure tool [1].

For the planned production at 32/22nm half-pitch node the substrate material has to reach an extreme flatness requirement of around 30nm which at the same time may not expand with rising temperatures in order to preserve pattern placement accuracy. While for the current generation of EUV alpha demo scanners the temperature of masks is quite comparable to classical 193nm masks, temperature as high as 50 to 80 degrees might be reached in high volume production tools [2]. The multi-layer mirror in conjunction with the absorber pattern will carry the required image of the final chip still with a 4x reduction in size during exposure. The multi-layer itself will have to have a reflectivity of about 67% with no embedded defects larger that 26nm [3]. The typical absorber for EUV masks consists of a TaN based material that needs to be as thin as possible to minimize shadowing effects due to the non-telecentric illumination in EUV scanners and yet be thick enough to provide the required optical density. Several types of absorber stacks have been proposed and tested in the last few years. The two major variants are i) a TaN-based absorber including an anti-reflective coating (ARC) on top of a buffer material and a Silicon cap over the multi-layer mirror and ii) a TaN-based absorber with ARC directly coated on a Ruthenium-capped multi-layer. The latter variant usually has a lower total height also allowing a very thin absorber with attenuated PSM type behavior.

The backside coating is required to insure a proper chucking to the electrostatic chuck in the exposure tool. Its parameters need to be compatible with the mask making and mask verification process.

Linked to the new materials are optical properties for the mask blank and patterned mask that might deviate from the known 193nm materials. While most tools can readily be employed for EUV mask making some tool support functionality is not yet available at the expected level. For example, several tools needed to be newly trained or even be modified to allow a proper detection of EUV mask positions or orientation, pattern recognition for alignment, and so on. For mask patterning and repair new recipes have to be created or chemistries be applied. For a few tasks totally new tools have to developed and integrated into the mask flow. The most prominent of such tools would be an EUV AIMS required for a characterization of the defect printability and final verification of a successful repair. This tool is seen by many people as mandatory for a viable production process.

Availability of high quality EUV mask blanks

A key ingredient from a mask maker’s perspective for the manufacturing process in a productive environment is the availability of adequate mask blanks. EUV blanks as described in the previous section have a very complicated stack composition with many production steps that could be prone to defect creation during blank manufacturing. The proper understanding of the defect creation mechanisms allows users to design manufacturing processes which minimize the occurrence of fatal defects – the ultimate goal in this area. However, the set of requirements on masks blanks which need to be reached at the same time has conflicting parameters that usually work against each other like polishing processes required for ultimate flatness create defects within the surface of the substrate ending up in phase defects, or substrate cleaning processes create voids in the surface [4]. Sematech at its mask blank development center has intensively studied these mechanisms and has cooperatively developed tools and processes with tool vendors and blank suppliers to foster the blank production. Despite the enormous progress made over the last few years the blank defect detection sensitivity on the different blank stack materials is not yet sufficient nor is the current defect level. A next generation blank defect inspection is required which might have to be complemented by an actinic blank inspection tool to locate multi-layer defects. Mask makers need to be prepared to base their mask manufacturing processes on blanks which are not completely defect-free and develop defect mitigation or masking strategies to finally deliver masks without printing defects. One necessary ingredient for this is a defect map (delivered to the mask house by the blank supplier) with exact coordinates of each blank defect. New concepts like mask blank identifiers [5, 6] and fiducial markers to span a coordinate system need to be introduced [7] and be standardized. Mask writing strategies have to be conceived that make use of these information to place e.g. defects under absorber structures or run dedicated repair or masking processes at the defect coordinates.

One of the problems of defect detection during the blank production process is the variety of different mask stack materials. Here the learning cycle could be drastically improved if the industry could harmonize on a limited or even unique set of materials. Once the absorber is deposited on the multi-layer stack, defects in this stack level or at the boundary to the substrate can no longer be detected by the usual blank inspection systems present at the mask house.

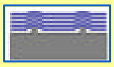
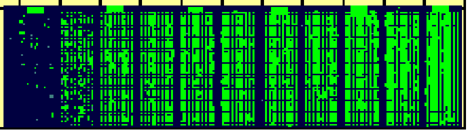
A second very important blank parameter is its flatness. The SEMI standard [8] specifies the largest deviation (peak-valley [pv]) of the substrate material from a perfectly flat geometry as the relevant parameter – values as low as 30nm pv are required for the production time. The polishing process effort necessary to get to these dimensions is exorbitant and hence the price of blank substrates becomes very high – maybe too high for a commercially viable mask manufacturing. Also in this area mask makers might be required to envision compensation mechanisms during mask writing that will take the effect of an imperfect shape of the blank into account during mask writing [9] by modifying positions where patterns are placed. Here as well as in the defect case the blank supplier would have to create a map with the measured flatness shape of the produced blanks and send this map with the blank to the mask maker.

Depending on the customer design the mask maker would now have to search in his inventory for an appropriate blank which matches best the customer requirements for flatness and defect location and start the mask manufacturing with the identified blank in the correct orientation to mask the majority or all defects and at the same time adjust the pattern placement for the flatness topography. This is a completely new way of operation in a mask house and the corresponding logistics within the supply chain and mask house operations still require major development work.

EUV mask manufacturing process

Part of the required infrastructure already exists at the AMTC. The reticle sorter was set up to identify automatically an EUV blank and depending on the material grade (engineering blank with quartz substrate and two notches vs. production blank with LTEM substrate and three notches) to correctly determine the required orientation of the blank for resist coating or writing. In conjunction with the blank serial number supplied within by the manufacturing information system, processes to make use of defect of flatness maps could be integrated.

To verify the quality of incoming EUV blanks or the resist coating an inspection is performed on the Siemens blank inspection tools DF40XP or DF70XP, respectively. The DF40XP tool was built by Siemens for the AMTC for the fast scanning of EUV blanks down to 40nm blank defects. Its performance is described elsewhere [10]; the second scan unit within the DF40XP or the standard DF70XP is used to verify the quality of the resist coating. Figure 1 shows results for a scan of a programmed defect blank (quartz bumps covered with multi-layers, blank kindly provided by Hoya) where the defects found in automatic mode are displayed as green dots. The sensitivity was increased compared to [10] by ramping up the laser power from 10% to 16% and several tool improvements implemented by Siemens during this year.

#	1	2	3	4	5	6	7	8	9	10	11	12	13
Defect width (nm FWHM)	70	80	90	95	100	110	120	140	150	160	170	190	300
Defect Height (nm)	1,0	2,0	2,8	3,0	3,2	3,3	3,6	3,6	3,8	3,8	3,8	3,8	3,8
ML Defect image 													

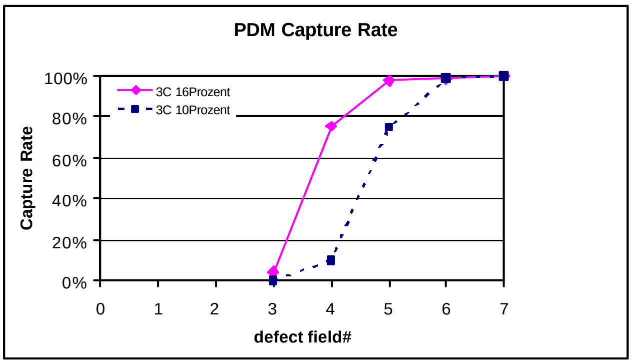


Figure 1: capture rate for defects on a programmed defect mask (quartz substrate bump defects covered with multi-layer). The dotted line represnts the setting from end of 2007, the solid line from end of 2008. The upper table shows the dimension of the automatically found defects.

After resist coating the blank is transferred to the e-beam writers in the required orientation. For standard optical masks the design data for the mask and the corresponding CD and placement correction maps are loaded and applied during writing. This could be enhanced for EUV masks to incorporate changes which depend on flatness or defect maps or on the material used. In the past the AMTC has primarily worked with the material stacks including buffer layer from Schott Lithotec [11, 12, 13] and Hoya, but now has the ability to also work with buffer-less materials from Hoya and Asahi.

It is obvious that the etching process is strongly dependent upon the material stack composition and dimensions, as well as that the achievable resolution depends on the resist type and thickness in conjunction with the resist consumption of the selected etch process. Figure 2 show an example of a contact hole arrangement of 80nm nominal size on one of our 2008 test masks.

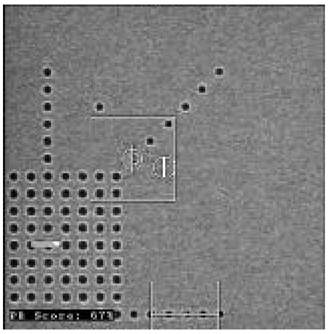


Figure 2: contact hole array resolved down to 80 nm on the mask.

Less obvious is the impact of the stack composition on the mask verification steps to follow. While the EUV mask materials show very similar and robust behavior at 13.5 nm and at the typical pattern inspection wavelength of 257 nm, their different response to other wavelengths or e–beams might become surprisingly important. Several tools needed an adjustment of blank detection and alignment units as well as a modification of the pattern identification and alignment. Likewise, the mechanical behavior of different material stack compositions has to be taken into account for pattern placement accuracy in any tool with a 3-point mount like in the e-beam writers or IPRO registration tools.

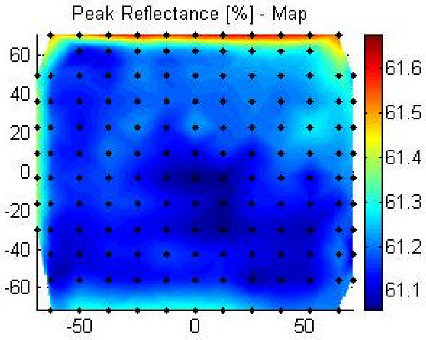


Figure 2. Reflectance uniformity measurement performed at the PTB

The etching and later the cleaning might change the optical properties of the capped multi-layer stack. One way to verify a good optical uniformity is to directly measure the reflectivity on the mask with an actinic reflectometer. AMTC in the past has made use of the EUV measurement capability at the synchrotron facility at the PTB in Berlin. Shown in figure 2 is an older result of a uniformity measurement performed during a cleaning impact study. Here we found for the engineering material studied that consecutive cleanings would change the reflectance less than 0.1% per cleaning cycle.

This year we have obtained the first results from a clean room size reflectometer demonstrator tool. Based on their previous blank inspection reflectometer tool AIXUV has started the development of the mask reflectometer with has a spot size small enough to measure on our standard test design. The construction work of this patterned mask reflectometer is supported within a joint project funded by the Germany Ministry of Education and Research [14]. First results from this tool will be reported at the EMLC 2009 in Dresden [15].

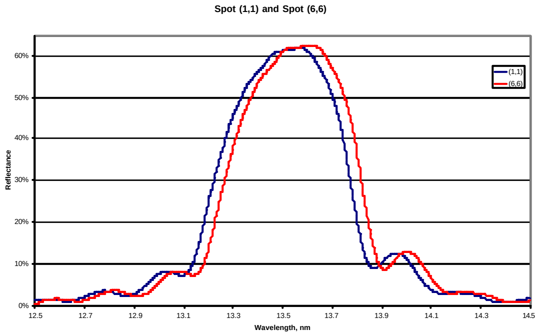


Figure 3 Reflectance measured with the AIXUV mask reflectometer test stand at two different locations on an engineering test plate.

EUV defect inspection and repair

With the KLA-Tencor 587 inspection tool the mask is being scanned for pattern defects. The standard settings allow a die-to-die inspection with the 72nm pixel (see figure 5 for an example of a particle defect found in die-to-die inspection), a die-to-database inspection capability is under installation. The inspection is able to locate classical pattern defects, particles, and to some extent also multi-layer defects. Defects have been studied extensively [16, 17, 18, 19] on recent EUV masks and compared to their printing image. Location of defects on the mask have been successfully determined with the help of repeater analysis on the wafer resist images [20] for masks that had a limited or no die-to-die inspection capable design. Different groups found different sensitivity levels and their conclusion therefore vary drastically with the respect to the severance of multi-layer defects.

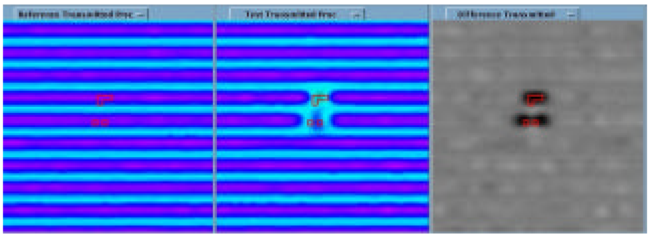


Figure 5: particle found in die-to-die inspection on KLA587

Figure 6 shows a selection of defects found on mask as well as on wafer. Two of these can clearly be identified as a pattern defect that can be repaired and as a particle contamination that can be cleaned away. The third defect is classified as a blank defect.

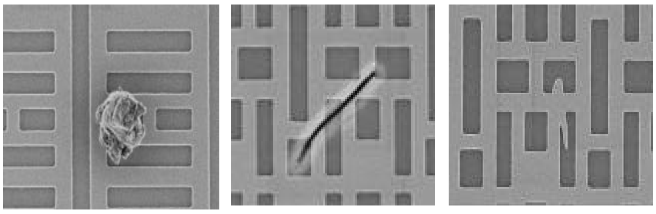


Figure 6: A selection of defects found on an EUV mask. On the left a particle is shown, in the middle a blank defect and on the right a pattern defect [17].

The forth defect shown here in figure 7 is quite peculiar and hardly visible in the SEM image, however, was clearly found on the wafer as a repeater and on the mask in the die-to-die inspection. An AFM scan revealed a dip in the surface of about 18nm depth and 130nm length. We interpret this as a multi-layer defect which shows up at the surface as a topography deviation. Further studies are required to check under which conditions multi-layer defects can be found by standard inspection tools or whether a true actinic inspection is required to locate all relevant multi-layer defects before conducting a printing experiment.

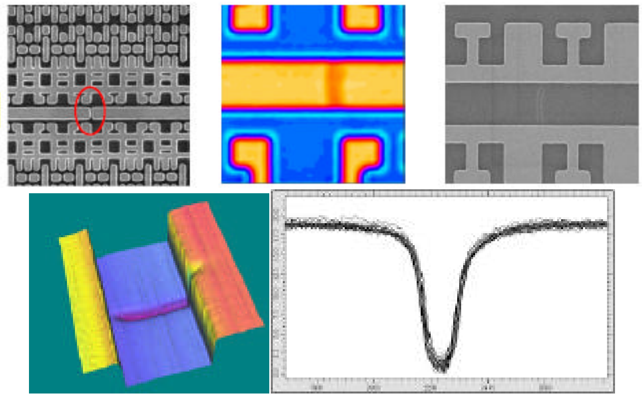


Figure 7: Possibly a multi-layer defect found by the standard die-to-die inspection. The left top shows the wafer image, the other two images on the top the inspection and SEM image. The lower row shows the result of an AFM scan on the mask.

Defects found in the absorber layer can be repaired either using a nanomaching device for removing dark defects or with an e-beam based etch- and deposition-tool. Figure 8 shows a repair performed on a pattern defect caused by a particle during the etching step. This repair has been successfully performed with the RAVE tool. On the right hand side the printed image after repair is displayed.

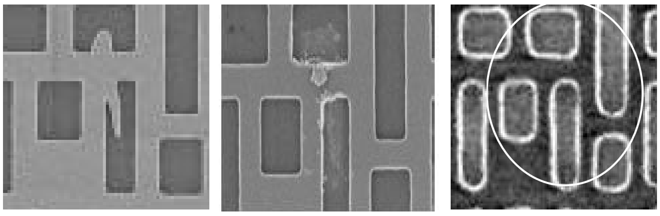


Figure 8: pattern defect before and after RAVE repair with its printed image after repair [17].

EUV mask transportation, handling, and contamination

Once the mask is properly finished and verified it needs to be transported o the point of use. Since an EUV mask is not covered with a standard pellicle (due to the absence of transparent films at 13.5nm wavelength) special care has to be exercised during transport and handling in the wafer fab. Extensive tests have been conducted with newly designed dual pod carriers [21,22,23]. Based on early work and experience a carrier based on the new SEMI 4466 standard have been produced, comprised of an inner pod to reduce the volume around the mask to minimize the risk of contamination and a slightly modified RSP like outer pod. This combination has been shown to not add any defects during transportation and storage and hence would be a viable carrier for the time of EUV production. In the mask house the infrastructure has to be adapted to make use of these carriers which resemble the usual SMIF pods used for regular mask manufacturing. However, the current infrastructure on the scanner side is not yet adapted to these new dual pods and manual handling is still required. During the usage of the mask in the scanner contamination with carbon might occur which need to be removed in order to preserve the full functionality of the mask. To determine the effect of massive contamination on printing experiments at the Berkeley MET have been performed with the contamination applied by the MIMICS tool at Albany. The mask has been contaminated with different levels of carbon thickness and printing results have been compared before and after cleaning [24]. The major observed effect is an increase of the dose to size which scales with the carbon thickness. The original behavior can fully be recovered after mask cleaning. For example the contrast of the cleaned fields has been shown to be identical to the reference fields by measurements at the AIT in Berkeley. Further studies, however, are required to determine the effect of multiple cleaning cycles on the lifetime of an EUV mask.

Conclusions

While much progress has been made over the last few years in the area of blank manufacturing and mask making, the path towards a fully defect free mask for a productive EUV lithography is still quite long. The defect sensitivity of blank and mask defect detection tools is not yet sufficient to allow blank and mask manufacturers to develop their respective processes to be defect free. Cooperative work along the supply chain including major research labs and organizations are still needed to make this technology a viable solution for future lithography. Promising results of these fruitful co-operations between the various players in the area of blank manufacturing and blank defect detection have been presented at recent conferences. However, there is still a lack of cooperation in the area of mask manufacturing across the global key regions despite promising first attempts.

Acknowledgments

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