Optimal Mask Characterization by Surrogate Wafer Print (SWaP) Method

Kurt R. Kimmel[1], Ingo Hoellein[1], Jan Hendrik Peters[1],
Paul Ackmann[2],
Brid Connolly[3], Craig West[3]

[1] Advanced Mask Technology Center GmbH & Co. KG, Raehnitzer Allee 9, 01109 Dresden, Germany
[2] Advanced Micro Devices, Inc., Sunnyvale, California, USA
[3] Toppan Photomasks Inc., Raehnitzer Allee 9, 01109 Dresden, Germany

Keywords: wafer print inspection, wafer level inspection, mask wafer correlation, indirect inspection

ABSTRACT

Traditionally, definition of mask specifications is done completely by the mask user, while characterization of the mask relative to the specifications is done completely by the mask maker. As the challenges of low-k_1 imaging continue to grow in scope of designs and in absolute complexity, the inevitable partnership between wafer lithographers and mask makers has strengthened as well. This is reflected in the jointly owned mask facilities and device manufacturers' continued maintenance of fully captive mask shops which foster the closer mask-litho relationships. However, while some device manufacturers have leveraged this to optimize mask specifications before the mask is built and, therefore, improve mask yield and cost, the opportunity for post-fabrication partnering on mask characterization is more apparent and compelling.

The Advanced Mask Technology Center (AMTC) has been investigating the concept of assessing how a mask images, rather than the mask's physical attributes, as a technically superior and lower-cost method to characterize a mask. The idea of printing a mask under its intended imaging conditions, then characterizing the imaged wafer as a surrogate for traditional mask inspections and measurements represents the ultimate method to characterize a mask's performance, which is most meaningful to the user. Surrogate wafer print (SWaP) is already done as part of leading-edge wafer fab mask qualification to validate defect and dimensional performance.

In the past, the prospect of executing this concept has generally been summarily discarded as technically untenable and logistically intractable. The AMTC published a paper at BACUS 2007 successfully demonstrating the performance of SWaP for the characterization of defects as an alternative to traditional mask inspection [1]. It showed that this concept is not only feasible, but, in some cases, desirable.

This paper expands on last year's work at AMTC to assess the full implementation of SWaP as an enhancement to mask characterization quality including defectivity, dimensional control, pattern fidelity, and in-plane distortion. We present a thorough analysis of both the technical and logistical challenges coupled with an objective view of the advantages and disadvantages from both the technical and financial perspectives. The analysis and model used by the AMTC will serve to provoke other mask shops to prepare their own analyses then consider this new paradigm for mask characterization and qualification.

1. Introduction

The microlithography stakeholders in the industry seek to determine the quality of a photomask by specifying many physical characteristics that have been carefully correlated to imaging results characterized in either resist or on etched

Photomask Technology 2008, edited by Hiroichi Kawahira, Larry S. Zurbrick,
Proc. of SPIE Vol. 7122, 712219 · © 2008 SPIE · CCC code: 0277-786X/08/$18 · doi: 10.1117/12.801685

wafers. The transfer functions involved in determining how the photomask characteristics interact with the scanner characteristics and the photochemical processes encompassed by the resist, create a myriad of complexities. This complexity, in conjunction with the angstrom-level magnitude of precision needed to make the overall analysis useful, makes the problem practically intractable. Numerical solvers of Herculean scope are marketed by various commercial suppliers to provide some approximation to the answer. However, the ultimate solution is the most straightforward technically but the least desirable culturally. To print the mask and characterize the wafer in all usual manners reduces the problem from a scientific search for mechanism to a practical evaluation of result. This work documents the analysis of the practical approach, putting aside the cultural bias against the method and exchanging (or swapping) the traditional evaluation of performance against physical mask specifications derived from complex transfer functions for direct assessment of capability.

2. Technical Aspects

The SWaP concept offers many technical benefits for characterizing the quality of a photomask while presenting some significant limitations and challenges to its use. The attractions and deficits associated with SWaP are summarized for clarity according to the following key mask quality parameter categories.

2.1. Critical dimension (CD) control

Traditional CD-SEM measurement provides good representation of a mask's mean deviation from nominal and its uniformity. However, the transfer function for CD between mask and wafer has many more variables (sidewall angle, MEEF, phase error, birefringence, depolarization, pellicle effects, etc), which produces a range of results and opportunity for multiple inexact conclusions. This non-specific result is important since it reflects the inherent instability of intertwined linear and non-linear multi-variant functions involved, and lends weight to the concept that the best way to assess mask CD performance on the wafer is to print a wafer. This circumvents the complexity of the functional description and goes directly to the result, which includes all imaging peculiarities in the imaging path and mask effects that are difficult to model. However, it is not perfect, in that the result produced is only valid for the specific set of conditions existing at the time of the wafer print. That is to say, a mask will print differently depending on the scanner used due to signature differences (focus and other aberrations, illumination/dose uniformity, polarization, etc.), the photoresist chemistry, the integrated process window, and the environmental conditions. This can be used to optimize mask level types with particular scanners and overlay signatures with particular wafer chucks. Determination of the necessary model inputs to achieve equivalent optimization by simulation would be exceedingly difficult at best.

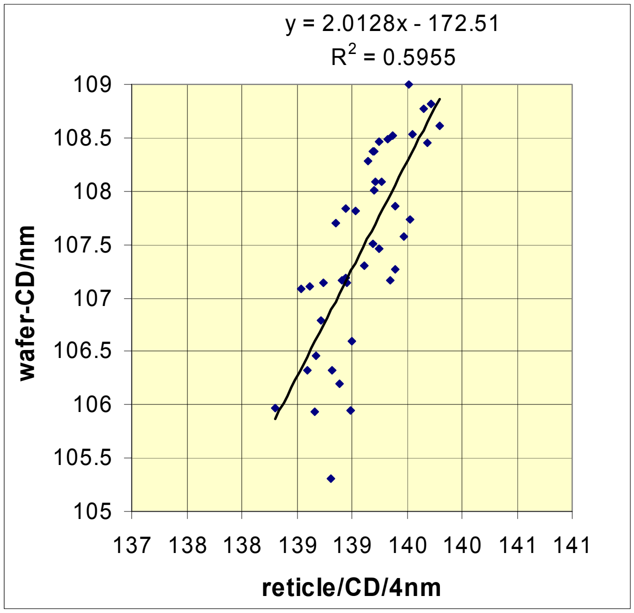


Fig. 1: Representative wafer vs. reticle CD scatter plot showing approximately 10 angstroms variation around the linear correlation fit with r2 = 0.6.

Figure 1 shows a reasonable correlation of mask and wafer CD, which is offered here as generally representative data from internal studies. However, the variation around the fit line of 10 angstroms range represents a significant portion of overall CD specification for advanced products that are, for example, 26 angstroms for critical levels and 13 angstroms for the gate level CDU 3-sigma for the 32 nm physical half-pitch node, according the 2007 ITRS. Recent work on the use of aerial imaging systems (AIMS), e.g., Zeiss AIMS^{TM} for mask CD measurement shows that this method is extremely well correlated with wafer print CD [7]. The maximum error was 4.4 nm (about 10%) but for an uncalibrated metrology tool measuring not exactly the same structures. The weakness of this method is that MEEF associated with the particular wafer resist contrast is not captured in the aerial image-based measurement.

With the introduction of CDU compensation technology using laser-induced substrate gray-scaling, e.g. Pixer^{TM} [8], the need for a wafer print to create the mask CDU signature correction file already exists. For a mainstream user of this CD Correction (CDC) technology, the incremental cost to use the same wafer verification print or one additional wafer printed at the same time for registration, pattern fidelity, and defect characterization becomes minimal.

2.2. Registration

The case for direct wafer measurement of mask distortion is similar to that for CD control. The correlation has been studied by the AMTC with collaborators. Wafer overlay between two masks is a function of multiple interacting factors from the scanner (aberrations, stage/scan control) and the wafer process, but is dominated by the mask registration. Currently, mask specifications are derived by conservatively budgeting the mask component of the overall contributions to wafer overlay to account for the scanner and wafer imaging factors' variations and metrology errors. Designers use different mask-versus-wafer budget ratios depending on product type and the layer feature types and their sensitivity to overlay error. Regardless of the mathematical methods or the design motivations, the budgeting process is necessarily biased to be conservative to compensate for the inaccuracies of simulation methods. This implies that, over a statistically significant population of manufactured masks, some masks with registration that are in reality satisfactory, will be scrapped. This may not be enough to justify the SWaP method but, again, it adds worth to the concept and to the argument for analysis of the option.

Work done by AMTC and its collaborators shows residual errors of approximately (x,y) = (8 nm, 20 nm) 3-sigma when two overlaid masks are subtracted from the overlaid wafers [5]. This is an indication that the transfer function is subject to influences that are not reflected in the mask registration metrology but are significant to the wafer overlay performance. In this case, the mask registration data and the wafer results are well correlated with coefficients (x,y) = (0.86, 0.94) but the magnitude of the stochastic scanner-cluster-induced error is quite high. The wafer results provide a much better characterization of the performance of the mask when considered as part of the whole imaging system: mask + scanner + wafer process.

Additional work done by AMTC and collaborators focused on characterization of mask issues with respect to double-exposure applications. In this work, both the correlation coefficient of mask versus wafer data at (x,y) = (0.79, 0.89) and the residual error at approximately 2 nm 3-sigma variation were quite good [4]. In this case with relatively small residual error, the wafer print overlay performance is an excellent reflection of the mask-measured data in both systematic signature and error magnitude.

2.3. Defectivity

This may sound like lithographic blasphemy, but the defects found on the mask are not what matters -- it is their printability that does. Therefore, defectivity characterization by traditional mask inspection methods can fail to be an optimum solution. Defects flagged may not print, or defects found may not be electrically pertinent to an active circuit. A most disturbing case is that some defects may print at 193 nm, given the particular illumination or focus conditions in the scanner, but not be found by the mask inspection system (whether it be actinic or not). Similarly, the SWaP method presents some significant limitations to its application. For example, SWaP cannot be applied to single-chip mask designs because the commercial wafer inspection systems use a die-to-die comparative inspection method. This becomes a boundary condition for a relatively significant proportion of logic mask designs. Second, there is no satisfactory method to distinguish between soft and hard mask defects by interpreting the wafer inspection data. Consequently, mask defect review becomes more cumbersome because all defect events found on the wafer need to be assessed and addressed with repair or clean.

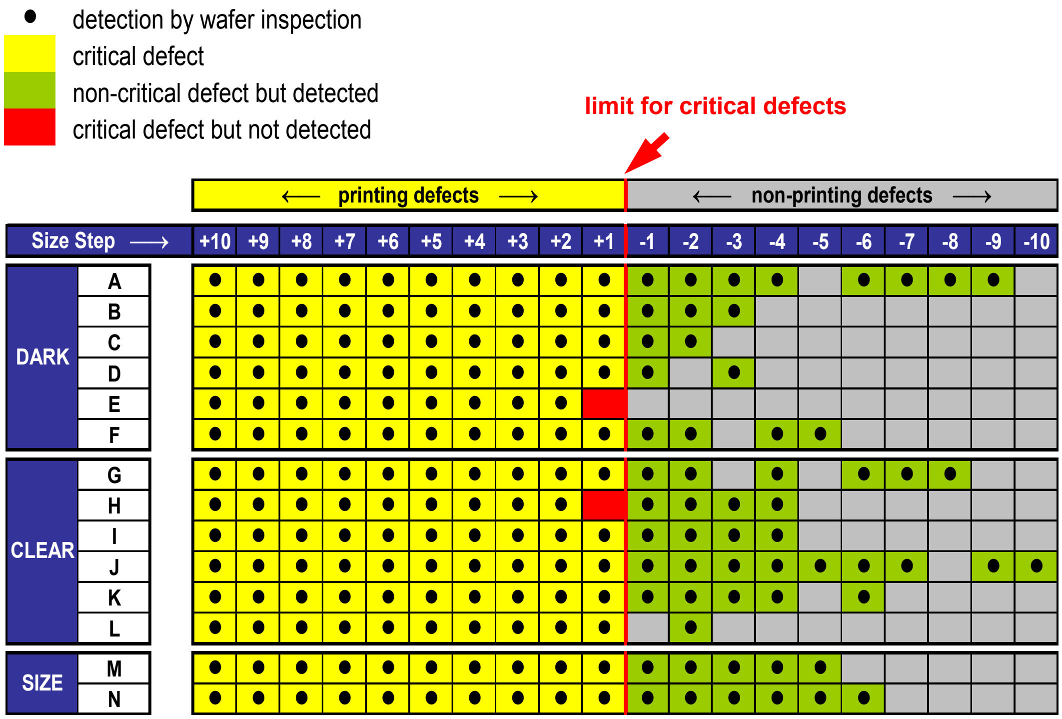
AMTC has investigated the use of SWaP specifically for defect characterization and reported this work at SPIE BACUS 2007 [1]. This work demonstrated, using a 65 nm DRAM test design as the vehicle, that direct mask inspection nominally captures more defects (critical and non-critical) than wafer inspection but, SWaP is more sensitive (defect size resolution) for some feature types and particularly for mis-sizing defects. With respect to the detection of critical printing defects, wafer inspection found all except for two in this evaluation. (marked by red cells in Fig. 2) However, these two were the smallest printing defects of two defect types (types E & H just adjacent the red line of printing criticality). For one of these two defect types, smaller but sub-critical printing defects were also detected which is not understood. This indicates a possible subtlety of the inspection setup causing this particular missed defect's scattering signature to not meet the detection threshold. The result constitutes feasibility of the method which can be improved with further inspection and wafer print recipe setups optimized for the purpose of revealing critical printing defects.

An important caveat associated with this work is that the mask inspection was done using a 90 nm pixel on a KLA 576, which does not represent the state of the art, and the wafer inspection using a KLA 28xx. However, for the demonstration product type used, the inspection sensitivities were appropriate.

This work was extended in 2008 to look at sub-50 nm hp DRAM and logic designs with the latest tool and pixel sizes, as well as extension to EUV [6]. In all cases, repeating defects located on the wafer print could easily be found on the mask and classified using SEM. (See Fig. 3)

2.4. Repair Verification

The SWaP method can provide an optimized verification of repaired defects. This application requires, however, at least one additional wafer print cycle since the mask would need a first-pass SWaP to find defects and a second-pass SWaP to verify them. Alternatively, SWaP could be used only as a final pass verification of repairs and pellicle mount defects in conjunction with traditional inspection. In this sense, the SWaP method is replacing a traditional aerial imaging (AIMS^{TM}) type verification system. This application could become compelling when no AIMS^{TM} tool is available with the required illumination settings of the scanner or when the mask imaging tool itself does not yet exist as in the case for EUV. However, the AMTC has never found a case where the AIMS^{TM} tool failed to correctly characterize a defect's printability under normal process conditions, and hence, a general superiority of SWaP versus AIMS^{TM} can not be concluded.



● detection by wafer inspection
🟨 critical defect
🟩 non-critical defect but detected
🟥 critical defect but not detected

limit for critical defects

		⟵ printing defects ⟶										⟵ non-printing defects ⟶									
Size Step ⟶		+10	+9	+8	+7	+6	+5	+4	+3	+2	+1	-1	-2	-3	-4	-5	-6	-7	-8	-9	-10
DARK	A	●	●	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	
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Fig. 2: Summary of wafer print (SWaP) vs. the print threshold (ref. [1]).

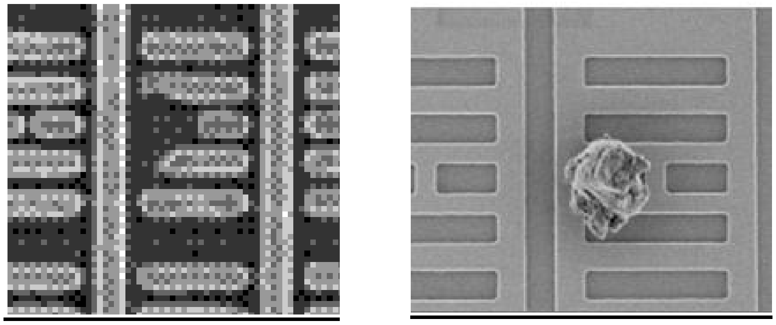

Fig. 3: Repeating defect found on wafer (left) and the corresponding mask SEM image (right).

2.5. Pattern fidelity

The subtle qualities of the image shapes on the mask can transfer to the wafer to cause significant yield loss due to process window contraction or electrical functional performance issues. Specifying mask corner rounding, line-end shortening, contact and via hole area, and line-edge roughness, due to complexities of how these features transfer through the wafer imaging system, presents a significant area of risky conclusions based sometimes on marginal metrology techniques. Since the scanner optics act as a spatial low-frequency band pass filter, many of the physical features on masks can be considered cosmetic defects. Discerning the boundary between cosmetic and harmful to create accurate shape fidelity parameters and specification is extremely difficult. As in the prior cases, the common treatment of this conundrum is to be conservative and specify statistically safe characteristics. That, again, implies mask yield loss is compensating for the conservative specifications, which are compensating for the inability to model the imaging transfer function accurately.

However, there is at least one commercial system available designed to fill the role of direct mask pattern fidelity inspection. It uses e-beam imaging to give the necessary resolution and compares the live image with the mask image rendered from the design data. Due to the raw pixel density of such an inspection, the throughput is relatively poor and the computing power needs are great.

The SWaP method alleviates -- again -- the capital investment and significant engineering overhead needed to maintain such a capability. The characterization of image fidelity is derived from two sources on the wafer: optical inspection and electrical measurement. Image fidelity issues large enough to trigger the defect thresholds come cost-free as a side effect of the normal wafer defect inspection. More subtle effects can be detected and assessed by studying the parametric data from electrical testing of kerf structures designed for this purpose. Since the electrical performance is the criterion that culminates all device manufacturing elements, including the mask, it makes it an ultimate quality measure but also presents challenges for separating mask-induced vs. non-mask-induced electrical observations. In this case, SWaP is not ideal but it may present the best alternative to address the issue.

3. Business Case and Logistical Issues

3.1. Mask CD/REG qualification metrology via wafer metrology

As explained in Section 2, there are many reasons to consider using just the wafer-printed image to characterize mask CD and registration performance rather than the direct mask measurements, which are redundant when considering that the wafer fab will qualify the mask again after reception. The reduction of redundancies between the mask qualification in the mask shop and the qualification in the wafer fab would bring advantages in cycle-time and costs, yet there is extensive utilization of CD and registration tools at both sites. The reasons for this lie in the timing of the availability of the metrology data. During the mask process development phase, the fast feedback loops are necessary to make decisions efficiently and correctly. Also, physical mask CD measurements are needed to create and calibrate wafer OPC models. Further, any mask shop needs to monitor its production process stability with SPC, and this is effectively and efficiently served by rapid direct mask physical measurements. For these reasons, the theoretical savings of direct mask CD and registration metrology equipment investments in favor of the SWaP method are missing. For the pattern fidelity application, the subtleties of the high spatial frequency feature attributes are most effectively checked with respect to their electrical performance impact. Characterization of repairs is done satisfactorily by the current aerial imaging tools.

With these boundary conditions applied to our SWaP analysis, the business case analysis space can be collapsed in scope to the primary technical application, which is defect characterization.

3.2. Mask defect qualification via wafer defect qualification -- business considerations

Figure 4 shows the mask defect verification flow. The left box describes the steps within the mask shop; on the right, the additional steps in the wafer fab are displayed. The standard flow is denoted by the black solid lines, the red lines show a potential SWaP flow. The dotted lines show the flow in case of repair and re-work. A pellicle would only be attached to the reticle for low-end products and COG masks, situations in which the first-time defect rate is negligible.

In a standard mask production flow, CD and registration measurements are done before defect inspection. Re-works or rejects due to CD and registration happen outside the discussed process flow and are, therefore, ignored in this discussion. Hence, yield-loss only takes into account the losses due to particles or defects that can be detected by either a traditional direct mask inspection tool (referred to as "standard-flow" subsequently) or a SWaP detection of a repeater.

In the following analysis, costs and cycle times for mask qualification have been compared for different scenarios described below.

On the wafer fab side, it is distinguished between a local versus a distant fab. This differentiation has a significant impact on the cycle time. For the local fab case (also used to represent the captive on-site mask shop case), shipping time from mask shop to wafer fab is assumed to be 1 hour (one-way). For the distant fab case, the shipping time is assumed to be 24 hours.

Further, it is distinguished between an engineering SWaP process flow (indicated as "Engineering" on the subsequent plot legends), which takes into account all time for litho cluster recipe set up and waiting in front of tools versus an optimized SWaP process flow (indicated as "Optimized" on the subsequent plot legends) in which these times are neglected for cycle-time calculations. In this case, it is assumed that the overall logistics and the process flow can be planned and executed in a way that the overhead steps can be done in parallel and neutralized relative to cycle time.

The last variable taken into account is the scanner utilization. This has an impact on the mask qualification costs. It is conservatively assumed that a mask qualification process via wafer print occupies the scanner cluster for 30 minutes. A dedicated scanner for mask qualification purposes only would have a capacity of approximately 48 prints per day. The costs calculations take into account the respective equipment costs (latest generation mask shop/wafer fab equipment), fixed costs, variable costs, facilities, and staffing (we neglected costs for mask shipping and raw wafers). The cycle-time calculations take into account raw process times, average waiting, and engineering times. The assumptions for the rework loops are derived from actual mask shop data. The reference mask product is a sub-65 nm DRAM/ 45 nm logic product mix.

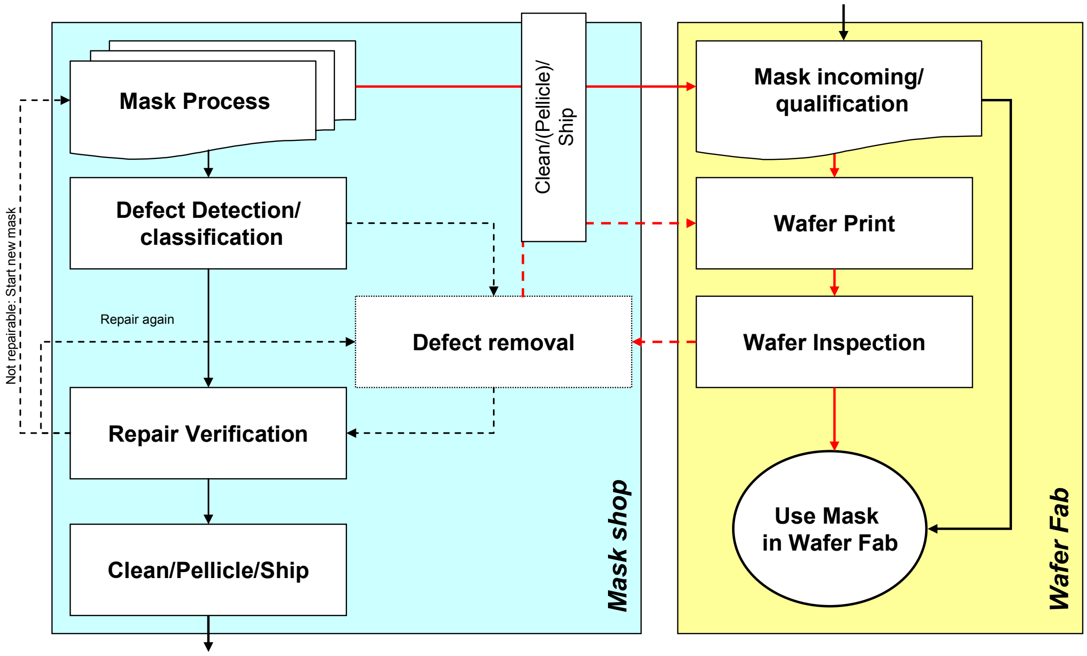

Fig. 4 Mask qualification process flow: standard-flow (black), alternative flow via wafer print (red); the doted line displays the rework loop

3.3. Cost Considerations

Our model for the mask qualification allows determination of the costs of the qualification as a function of the mask production line yield for the standard flow versus the SWaP flow with three different scanner utilization assumptions. The differentiation between local and distant fab does not make a difference here because the mask shipping costs are negligible relative to total cost. We have assumed a $50 million investment for a high-end scanner, track, and wafer inspection tool versus a $35 million investment for a high-end mask inspection tool. (These costs are estimates gathered from literature and unofficial reports. They do not reflect actual costs obtained by the AMTC or its partners.) From a mere cost perspective, mask qualification via wafer print is generally the cheaper option, driven largely by the wafer scanner and inspection tools' throughput compared to mask direct inspection throughput. A scanner utilization of only 25% is already sufficient to beat the standard flow reference case. This makes the argument for a scanner in the mask shop plausible, since it is unlikely that most mask shops could utilize the full capacity of a SWaP-dedicated scanner.

Note that our approach differs from scenarios that other authors followed. Dayal *et al.* focus on mask contamination during its lifetime in the wafer fab and accordingly, only consider particle contamination inspection based on the corresponding direct mask inspection tools [2]. Using $14 million for the scanner and track and 25% of this for the mask defect inspection tool, they conclude a lower cost associated with direct mask inspection over a wafer print-based inspection. This is a valid conclusion since a contamination inspection tool is cheaper by ~2X and faster by ~2-4X than a mask defect inspection tool with suitable performance to find hard defects with sensitivity commensurate for the technology node under test.

Battacharyya *et al.* built an elaborate model to calculate the opportunity cost induced by print verification of masks during their lifetime in the wafer fab [3]. Assuming a $25 million scanner track combination and 6 minutes of exposure tool time, they show that print verification is three times more expensive than the direct mask inspection. In a 15,000-wafer-starts-per-month fab, they predict lost productivity of about 500 wafers a year for 10 print verifications per day and about 4,000 wafers a year for 30 print verifications per day. Since the most attractive implementation concept is to apply the SWaP method for newly built high-end masks only, the final impact on wafer productivity would be minimal (less than 100 wafers per year using the Battacharyya *et al.* figure referenced), while the effectiveness in reducing advanced mask inspection investment would be optimized. We consider the wafer productivity loss to be negligibly small (less than 0.1% of wafer capacity) in our implementation model. Furthermore, for the implementation case of the SWaP scanner being inside the mask fab dedicated to mask characterization, the opportunity cost is zero.

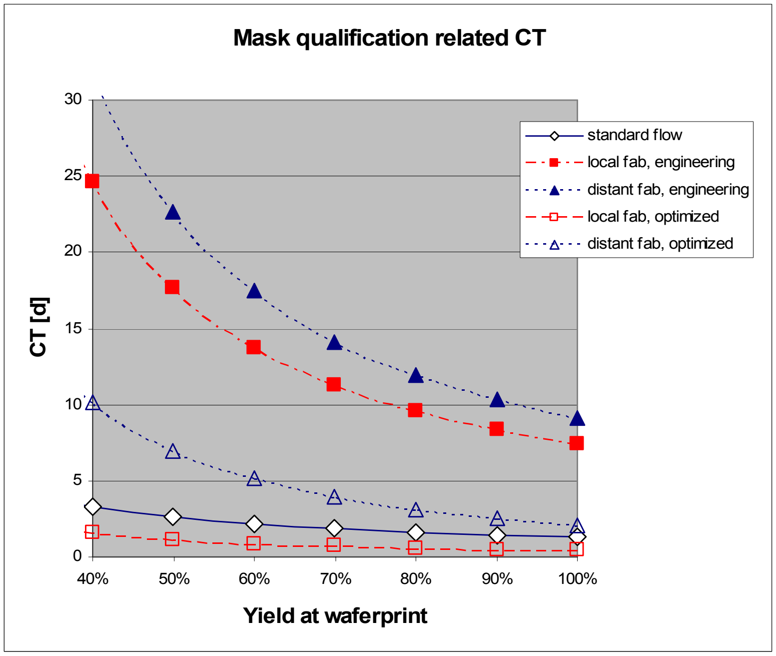

Fig. 5: Mask qualification cycle-time as function of yield: standard flow versus alternative flows (local vs. distant fab, engineering vs. optimized logistics flow).

Work published by Poock *et al.* shows comparisons of direct mask inspection with wafer prints [9]. Both methods found all the defects that matter except for a case in which wafer inspection did not capture dense area tip-to-tip defects. The authors note that, due to sensitivity gaps, a combined approach may be the optimal solution. They also concluded that cycle time could be relatively neutral for an optimized process, but opportunity cost for scanner time spent on mask qualification would be significant. However, no cost analysis comparing the two methods was given in this work. Our paper seeks to fill some of the gaps and bring analysis to the speculations by Poock *et al.*

3.4. Cycle time considerations

In the cycle-time comparison, the SWaP scenarios in general do not perform that well. Only the optimized logistics case with a local wafer fab can surpass the standard flow. Especially for lower mask yields, the cycle times explode due to repair loops and their related shipping times. Even with a line yield of 80%, which is rather optimistic for the most advanced mask products, and a local wafer fab customer available to engage in SWaP, the mask qualification cycle time would be nearly six times higher compared to the standard flow.

A new perspective on the different scenarios is given by plotting mask qualification costs versus mask qualification cycle times for different mask yield assumptions (see Fig. 6). This plot presents a summary of the application space for SWaP as a function of the most important variables individual readers will want to modulate. The plausible application space is quite small, driven by the cycle time issue associated with efficient execution of the actual wafer-printing step. However, the cases of a local fab (or captive local mask shop) and 100% scanner utilization with poor mask yield of 20%, or poor 25% scanner utilization with a mask yield above 80%, produce a viable case for SWaP.

3.5. Technical challenges for implementing mask qualification via wafer print

While we have shown that, from the cycle time and also from the cost point of view, SWaP might be favorable under certain boundary conditions, there are still a number of issues that need to be studied more carefully. Some of these topics are fundamental problems like one-die reticles that cannot be assessed currently with this method. Others are more logistical and risk-assessment types, like the additional contamination due to repetitive transport between mask house and wafer fab. Another caveat is associated with a new mask technology node development phase in which new wafer process and litho settings would have to be determined for each new mask material being investigated.

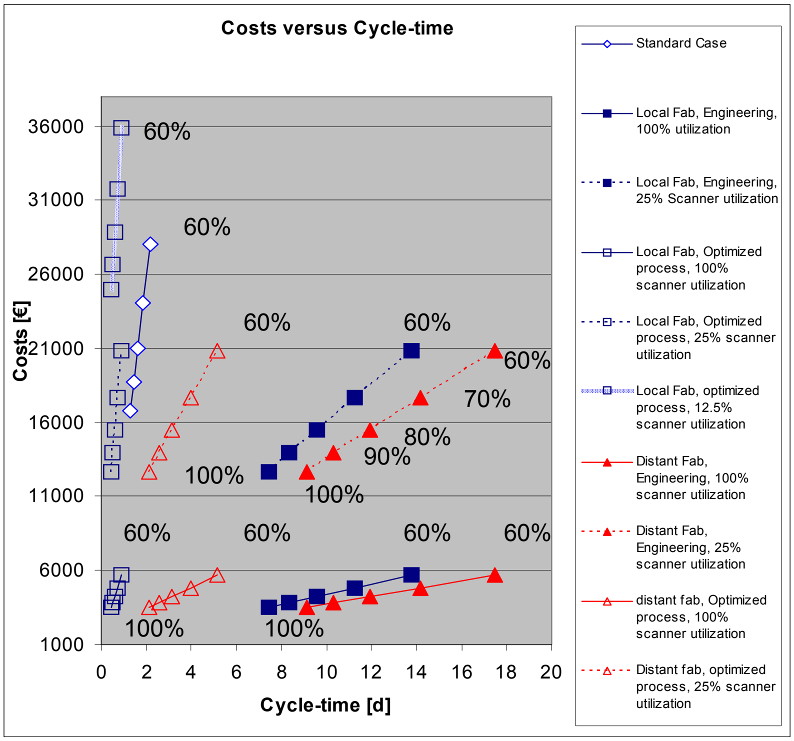

Fig. 6: Mask qualification costs versus cycle time for different mask yields ranging from 100% down to 60%

4. Strategic Approach

Taking into account the technical challenges described in the preceding paragraph, the authors provide the following SWaP application scenarios for consideration and further development.

4.1. SWaP implementation in local fabs

The most straightforward implementation of the SWaP concept is in conjunction with neighboring wafer fabs. This would essentially eliminate the cycle time overhead due to shipping as predicted by our model (see Fig. 6) and would lead to a minimal impact on the wafer productivity as predicted by Bhattacharyya *et al.* [3], since the number of newly built high-end masks delivered per customer per day is small.

4.2. SWaP implementation with dedicated scanner

The more daring proposal is the one of a scanner dedicated for mask verification. As we have shown, the capacity of such a scanner fully loaded with mask verification jobs -- even under our conservative assumptions -- is much higher than needed for all the high-end masks produced per day at a typically sized mask shop. However, our model predicts that even a utilization of only 25% would be sufficient to create a positive business case for such a solution in our environment. The residual scanner cluster capacity could be effectively utilized by wafer R&D efforts of neighboring wafer fab engineers. This type of partnership could provide an optimized solution, especially for the case of a captive on-site mask shop, and could promote further wafer lithographer / mask maker interactions.

5. Conclusions

This paper reported the likely benefits and deficits of using the characterization of a wafer print as a surrogate for direct mask characterization. The issues related to technical justification, cost comparison, cycle time impact, and implementation scenarios were discussed. The fundamental conclusions are summarized here:

- SWaP has technical justification for many mask characterization applications including CD, registration/ overlay, repair verification, and defect characterization. However, single die masks currently cannot be candidates for SWaP and wafer print defects are not easily classified with respect to their mask origin.
- SWaP has business justification only for defect characterization. (Note the important assumptions made as outlined in section 3.3.)
- SWaP has logistical justification only for the scenario of a wafer fab with local mask fab (captive or not).

The more plausible SWaP implementation scenarios are:

- Local mask fab (meaning less than one hour delivery time) with a non-dedicated scanner but optimized logistical system to execute SWaP; or,
- Mask fab with dedicated local or in-house scanner utilized more than 25%.
- Mask fab with dedicated local or in-house scanner shared with the wafer fab for wafer development purposes.

In some limited cases, the consideration of SWaP for implementation has additional compelling justification. For example, users of CDC (as developed by Pixer Corp., for example) have even lower incremental cost to implement SWaP since they may print a mask to provide a correction file anyway. The same wafer could be used for multiple wafer-level characterization purposes. In the case of EUV masks, SWaP is particularly compelling since no production-worthy AIMS-like tool or phase defect inspection capability exists.

The model and analysis presented here are meant to provoke other mask shops to prepare their own analyses with their own assumptions and engage their wafer fab partners in drawing conclusions.

6. Acknowledgements

AMTC is a joint venture of Toppan Photomasks, Qimonda, and AMD and together with AMD gratefully acknowledges the financial support by the German Federal Ministry of Education and Research (BMBF) under contract number 13N9675 and 13N9672 (ANTARES) and by the Free State of Saxony in the framework of the technology grants based upon European Regional Development Funds and funds of the Free State of Saxony under contract number 12707/2109 and 12734/2109 (Koala).

The authors are grateful for the contributions to the content of the paper made via discussions and/or data by Christian Holfeld of AMTC; Anna Tchikoulaeva, Stefanie Maelzer; and Rolf Seltmann of AMD; and, Claudia Grosser, Florian Uhlig, Arno Wehner, and Gerd Unger of Qimonda.

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