SiO_2 Buffer-Etch Processes with a TaN Absorber for EUV Mask Fabrication

Florian Letzkus[*a], Joerg Butschke[a], Corinna Koepernik[a],
Christian Holfeld[b], Josef Mathuni[c], Lutz Aschke[d], Frank Sobel[d]

[a] IMS Chips, Allmandring 30a, 70569 Stuttgart, Germany
[b] Advanced Mask Technology Center GmbH, Rähnitzer Allee 9, 01109 Dresden, Germany
[c] Infineon Technologies AG, Balanstr. 73, 81541 Munich, Germany
[d]Schott Lithotec AG, Otto-Schott-Str. 13, 07745 Jena, Germany

ABSTRACT

Extreme Ultraviolet Lithography (EUVL) is the favourite next generation lithography candidate for IC device manufacturing with feature sizes beyond 32nm.
The SiO_2 buffer dry etching is a crucial step in the manufacture of the EUV mask due to stringent CD- and reflectance requirements. In contrast to conventional chromium absorber layers new absorber materials e.g. TaN require an adjustment of the SiO_2 buffer etch chemistry and process parameters to avoid a strong influence on the initial absorber profile and thickness.
We have developed a SiO_2 buffer dry etch process that uses the structured TaN absorber as masking layer. A laser reflectometer was used during the SiO_2 dry etch process for process control and endpoint detection.
Different dry etch processes with SF_6/He, CF_4 and CHF_3/O_2 etch chemistry have been evaluated and compared with regard to TaN- and SiO_2- etch rate, TaN- and SiO_2 etch profile and Si capping layer selectivity. We focused our work on minimum feature sizes and simultaneous etching of different line (e.g. dense- and isolated lines) and hole patterns. Line and contact hole structures with feature sizes down to 100nm have been realized and characterized in a SEM LEO 1560.
The whole mask patterning process was executed on an advanced tool set comprising of a Leica SB 350 variable shaped e-beam writer, a blank coater Steag HamaTech ASR5000, a developer Steag HamaTech ASP5000 and a two chamber UNAXIS mask etcher III.

Keywords: EUV, mask, dry etch, TaN absorber, SiO_2 buffer

1. INTRODUCTION

In contrast to conventional photomasks EUV masks are used in a reflective mode and, accordingly, they have a completely different configuration. A stack of Mo and Si layers coated on a low thermal expansion substrate provides the needed reflectance for the 13,4nm EUV radiation. A thin Si or Ru capping layer for Mo/Si multilayer protection is on top of the multilayer stack followed by a buffer and and absorber layer. Beside the function as etch stop for the absorber etch process, main task for the buffer layer is the protection of the Mo/Si multilayer mirror during the repair of absorber defects with a focused Ga^+ ion beam. Therefore a minimal buffer thickness of 40-60nm is required to avoid the penetration of the Ga^+ ions into the Mo/Si multilayer resulting in reflectivity changes. New e-beam repair methods of the absorber which would not need a special buffer layer are currently under investigation for EUV masks but still no final decision is fixed [1].
Different buffer layer materials eg. thin films of sputtered Cr or SiO_2 and different buffer wet and dry etch processes have been reported in literature [2,3]. We investigated the dry etch behaviour of a 60nm sputtered thin SiO_2 film with a TaN absorber as masking layer. Interferometric thickness measurements and SEM cross-section measurements have

[*] Letzkus@ims-chips.de, phone: +49-711-21855-451, fax: +49-711-21855-111

been carried out to examine the etch profile and process selectivity to the TaN absorber and Si capping layer. In addition EUVL test masks for exposure experiments have been fabricated and characterized with a CD SEM.

2. EXPERIMENTAL

For the SiO_2 dry etch process development two different test pattern for profile/selectivity determination and CD uniformity measurements have been designed. The profile/selectivity pattern comprises of the following modules which are arranged in a cross shaped matrix:

- dense and isolated lines of different line width (60nm-500nm) for investigation of line profile cross-section;
- contact hole arrays of different width (125nm-750nm) for investigation of hole profile cross-section;
- a 3mm x 3mm square for laser endpoint detection during the dry etch processes.

The CD uniformity pattern with a pattern density of 22% comprises:

- uniformity structures in an 11 x 11 array of 150, 250, 400, 600 nm dense and isolated lines covering the mask quality area of 130mm x 130mm;
- dummy pattern in between the uniformity structures for a pattern coverage of 25%;
- arrays of 49 square measuring points, exposed with an increasing dose for determine the resist sensitivity and contrast.

The resulting density of the CD uniformity test pattern is ~22%.

The dry etch process development was performed on 6 inch/250mil masks and on wafer substrates which have been mounted on top of a mask blank. This was a cheap and easy method to determine the Si and SiO_2 etch rate of different buffer etch chemistries and conditions. Thermal oxidized wafers and SOI wafers with a poly silicon layer on top of the oxide layer have been used. In respect to the achieved selectivity results on the wafer substrats the best buffer etch processes have been applied on TaN mask blanks to determine the selectivity and impact on the TaN absorber. Table I summarizes the used blank and wafer material for process development with the different layers and layer thicknesses.
Finally the best process was chosen for the fabrication of multilayer exposure testmasks (Fig. 1).
For mask coating positive tone chemically amplified resist FEP 171 (Fuji) was used [4]. The mask blanks were exposed with the variable shaped e-beam write Leica SB350 MW which operates at 50kV acceleration voltage with a beam current of $10A/cm^2$. This pattern generator fulfills the requirements of the 100nm technology node. After post exposure bake on a zone controlled hotplate the mask was developed with a TMAH based developer (TOK NMDW) in a 3x puddle process.
The absorber and buffer etch process development was accomplished with a two chamber UNAXIS mask etcher III. Both chambers for SiO_2 and TaN etching were supplied with an optical laser system for endpoint detection, operating at a wavelength of 673nm. SiO_2 and Si thickness measurements before and after absorber/buffer etch were performed on a LEITZ MPVSP optical interference microscope.
All CD measurements and investigations of cross-sections were done in a LEO1560 SEM.

3. RESULTS AND DISCUSSION

3.1. Etch rate determination

Prior to etch experiments with mask material the Si and SiO_2 etch rate for different SiO_2 buffer etch chemistries e.g. SF_6/He, CF_4, CHF_3/O_2 and process conditions has been measured on wafer substrates to evaluate the selectivity, which is one important criteria for an efficient buffer process. Therefore a $1cm^2$ big piece of a thermal oxidized wafer and of a SOI wafer was mounted in the centre of a TaN/Qz mask and has been etched. The SiO_2 and Si layer thickness has been measured before and after etching with an optical interference microscope.

The dependency of the SiO_2/Si etch selectivity for a constant CF_4 gas flow and different RF/ ICP power from pressure is diplayed in figure 2. For 100W RF power on the electrode the selectivity is independent whether the ICP source is turned on or off, furthermore the pressure dependency is very week. An addition of 5sccm does not improve this result.
The best process conditions for the CF_4 chemistry has been reached at a RF power of 200W with ICP source on. The process P1 has a SiO_2/Si selectivity of 1,16 and the process P2 of 0,89.
Figure 3 displays the SiO_2/Si selectivity for the addition of CF_4 in a CHF_3/O_2 plasma. Pressure, CHF_3/O_2 gas flow and RF power have been kept constant. The decrease of the Si/SiO_2 selectivity with increasing CF_4 gas flow shows an almost linear behaviour. The best process P3 with no CF_4 addition has a SiO_2/Si selectivity of 1,13.
The changing of the O_2 gas flow for a constant pressure and CHF_3 gas flow results in a significant drop of the SiO_2/Si selectivity from process P4 to P3 and P5 (Fig. 4). The best process P4 with no O_2 addition has a SiO_2/Si selectivity of 2,6.
The different etch processes P1-P5 with the best SiO_2/Si selectivity have been applied on mask substrates (mask blank II, s. table 1). The TaN etch rate of these buffer etching processes was measured from SEM cross-sections and the SiO_2 etch rate was calculated from the laser endpoint signal.
The SiO_2/TaN selectivity results are summarized and compared with a standard SF_6/He quartz etch process (Process P6) for phase shift mask making with a Cr hardmask (Table 2). A strong difference specially in the SiO_2/TaN selectivity for the SF_6/He process and the polymer building CF_4 and CHF_3 processes has been measured.
The etch profiles after absorber and buffer etching of the P1, P2 and P3 processes are shown for 125nm dense lines in the figures 5, 6, and 7. A rounding at the TaN absorber edge and a non vertical profile is for all three different processes clearly visible.
The best results have been achieved with process P5. In figure 8 is a SEM cross-section of the TaN profile for 125nm isolated and dense lines after the absorber etch process. These reference pictures were achieved on a mask which have been buffer etched with the P5 process by covering the structures with a thin capton-foil during buffer etching. In figure 9 and 10 cross-section SEM pictures of dense line, isolated line and contacthole structures on this specific mask are displayed after the P5 buffer etching process. A nearly vertical etch profile in the absorber was observed and no difference in the thickness of the Si layer for the dense isolated line and contacthole structures could be measured. This demonstrates that the RIE is not an issue for this P5 buffer etching process.

3.2. CD Uniformity

CD uniformity measurements after the absorber and buffer etch process have been executed at 150nm dense lines in the uniformity test pattern described in section 2. Within the 150nm dense lines the space was measured. The CD analysis of the SEM pictures was done with the linewidth measurement software from SIS (Soft Imaging System). The overetch for the TaN absorber was 50% of the main etch step[4]. For the SiO_2 buffer a soft landing step was executed after reaching the Si capping layer.
Figure 11 shows the achieved result after TaN absorber etching. A 3σ deviation of 11,9nm was obtained. After the SiO_2 buffer etching a 3σ deviation of 11,1nm was measured, which indicates the very low influence of this process (Fig. 12). The signature of the two uniformity plots also assists this result. A comparison of the CD mean values of both etch processes reflects a feature size shrinking after the buffer process of about 13nm. One possible explanation for this result would be the builtup of a teflon like C_xF_y sidewall polymer during buffer etching. Otherwise a small change of the absorber edge angle after buffer etching could influence the secondary electron emission signal at this position during CD measurement and therefore the CD measurement result.
Further investigations will explain whether a polymer sidewall deposition or a measuring artefact is the reason for that result.

3.3. EUVL Testmask Fabrication and Characterization

According to the developed buffer etch processes multilayer test masks for EUVL exposure experiments at the MET (Micro Exposure Tool) in Berkeley/USA have been fabricated. A real device pattern with 150nm poly gate similar structures could be realized showing the potential of the whole patterning process (Fig. 13).
CD measurements after absorber and buffer etch have been carried out for process characterization of this test mask. Dense lines and isolated spaces with feature sizes from 1600nm down to 100nm have been measured (Fig 14). Very good linearity results, 8nm for dense lines and 14nm for isolated spaces have been achieved (Fig 15, 16). The e-beam writing of these features was done with a non optimized proximity correction which indicates further potential for future

linearity improvements. Again a linear shift, specially for the isolated spaces, between the absorber and buffer etch off target values was observed.

4. CONCLUSION

Different etch chemistries for SiO_2 buffer etching with a TaN absorber have been evaluated on wafer and mask substrates. The achieved Si and SiO_2 etch rates on these two substrates were comparable, therefore selectivity experiments on cheap wafer substrates can be carried out and afterwardst transferred on mask blanks.
The CF_4 etch processes obtained a sufficient SiO_2/Si selectivity but high TaN etch rates. Processes with CHF_3/O_2 chemistry showed a better SiO_2/TaN selectivity and did not affect the absorber profile. With the best process (process P5) a SiO_2/Si selectivity of 1,44 and SiO_2/TaN selectivity of 7,5 has been achieved. SEM cross-section of 125nm line and hole pattern showed a vertical etch profile in the SiO_2 buffer and no footing or residues at the SiO_2/Si layer interface.
CD uniformity measurements after absorber and buffer etching at 150nm dense lines covering the mask quality area of 130mm x 130mm in a 11 x 11 array demonstrated now influence of the buffer process on uniformity, but a shrinking of the feature size of about 13nm, which have to be analyzed in the future.
Efficient test masks for exposure experiments at the MET with 100nm minimum feature size for dense lines and isolated spaces and 150nm poly gate similar pattern have been fabricated and characterized. For 1600nm-100nm pattern width a linearity value of 8nm for dense lines and 14nm for isolated spaces has been obtained.

5. ACKNOWLEDGMENTS

This work has been supported by MEDEA$^+$, Project: EXTUMASK, the German Federal Ministry for Education and Research, (contract sign 01 M 3064a and b) and by the Ministry of Economic Affairs of Baden-Wuerttemberg. The authors alone are responsible for the content.

REFERENCES

1. V.A. Boegli, K. Edinger, M. Budach, O. Hoinkis, B. Weyrauch, H.W.P. Koops, J. Bihr, J. Greiser “Application of electron beam induced processes to mask repair”, Photomask Japan 2003, Yokohama, Japan, April 16 -18, 2003
2. E. Hoshino, T. Ogawa, M. Takahashi, H. Hoko, H. Yamanashi, N. Hirano, A. Chiba, M. Ito, S. Okazaki “Process scheme for removing buffer layer on multilayer of EUVL mask”, Proceedings of SPIE 4066, Photomask and Next Generation Mask Technology VII, pp. 124-130
3. P.Y. Yan, A. Ma, Y.C. Huang, B. Stoehr, J. Valdivia “EUVL lithography square mask patterning with TaN absorber”, 1. International EUV Lithography Symposium, Dallas, USA October 15-17, 2002
4. M. Irmscher, D. Beyer, J. Butschke, C. Constantine, T. Hoffmann, C. Koepernik, C. Krauss, B. Leibold, F. Letzkus, D. Mueller, R. Springer, P. Voehringer, “Comparative evaluation of e-beam sensitive chemically amplified resists for mask making”, Photomask Japan 2002, Yokohama, Japan, April 23 -25, 2002.
5. F. Letzkus, J. Butschke, M. Irmscher, F.M. Kamm, C. Koepernik, J. Mathuni, J. Rau, G. Ruhl “Dry etch processes for the fabrication of EUV masks”, Microelectronic Engineering 73-74 (2004), pp. 282-288

Substrate	Layer stack	Layer thickness
Mask blank I	Qz/TaN	d_{TaN}=80nm
Mask blank II	Qz/Si/SiO_2/TaN	d_{Si}=80nm, d_{SiO2}=60nm, d_{TaN}=80nm
Wafer I	Bulk Si/SiO_2	d_{SiO2}=1000nm
Wafer II	Bulk Si/SiO_2/Si	d_{SiO2}=100nm, d_{Si}=200nm

Table 1: Mask blanks and Si wafers for process development

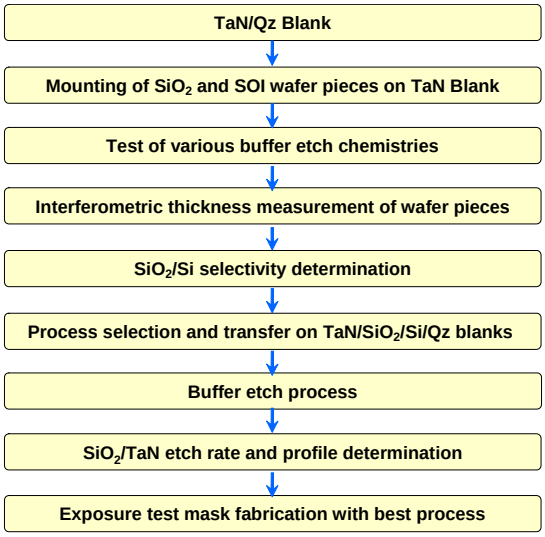

Fig. 1: Si, SiO_2 and TaN etch rate determination

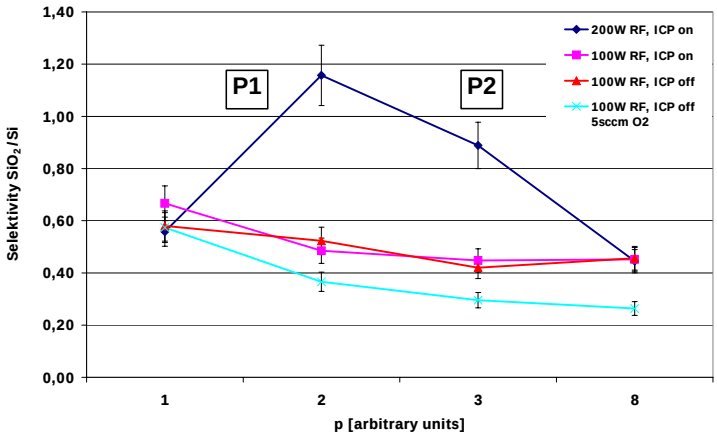

Fig. 2: Dependency of SiO_2/Si etch selectivity on pressure for a constant CF_4 gas flow

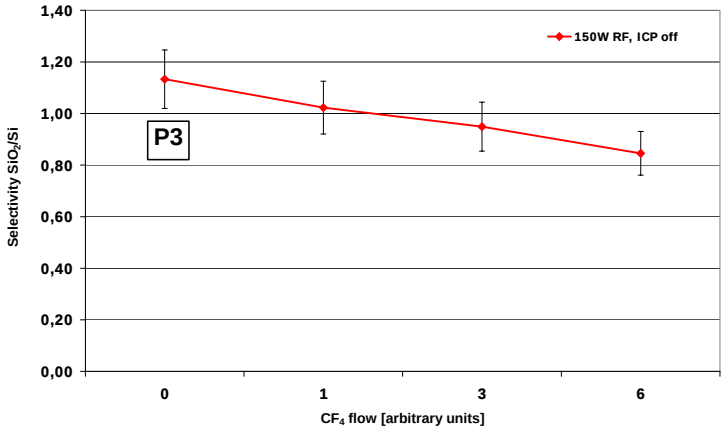

Fig. 3: Dependency of SiO_2/Si etch selectivity on CF_4 gas flow for a constant pressure and CHF_3/O_2 flow

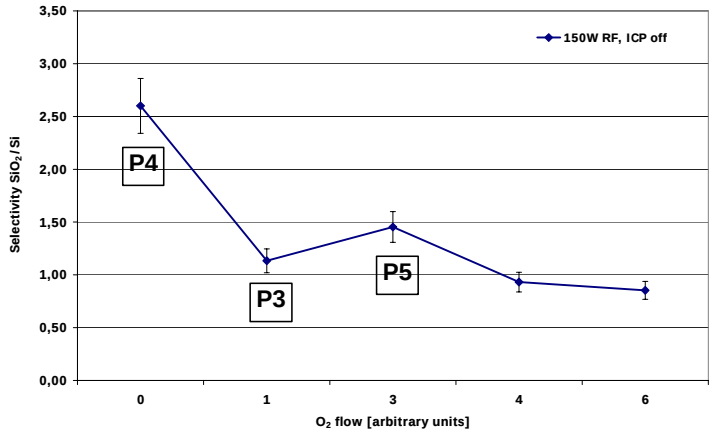

Fig. 4: Dependency of SiO_2/Si etch selectivity on O_2 gas flow for a constant pressure and CHF_3 flow

Process	Chemistry	Thermal SiO_2 etch rate on wafer substrate [nm/min]	Sputtered SiO_2 etch rate on mask substrate [nm/min]	TaN etch rate [nm/min]	Selectivity SiO_2/TaN
P1	CF_4	14,7	15	4,7	3,2
P2	CF_4	14	13,3	3,8	3,5
P3	CHF_3/O_2	8,5	6	1	6
P4	CHF_3	7,8	5,5	2,6	2,1
P5	CHF_3/O_2	7,7	6,2	0,8	7,5
P6	SF_6/He	15	14,5	23	0,6

Table 2: Etch rates of the different buffer etch processes

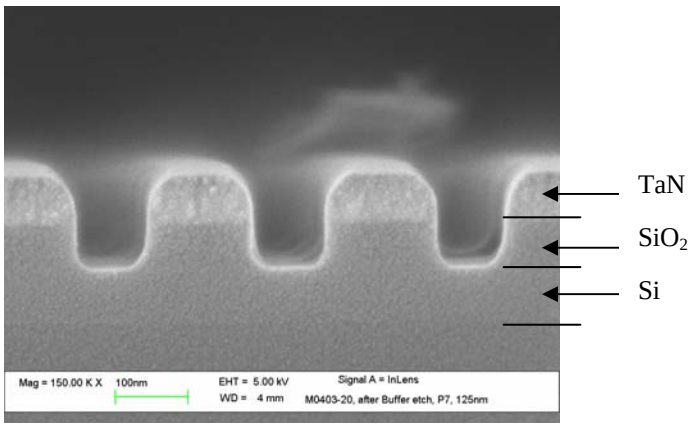

Fig. 5: P1, 125nm dense lines after absorber and buffer etching

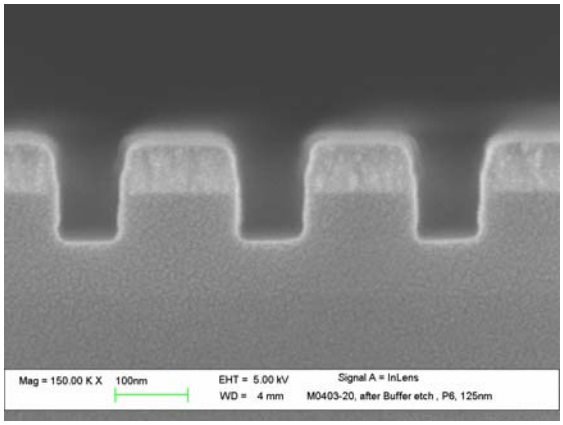

Fig. 6: P2, 125nm dense lines after absorber and buffer etching

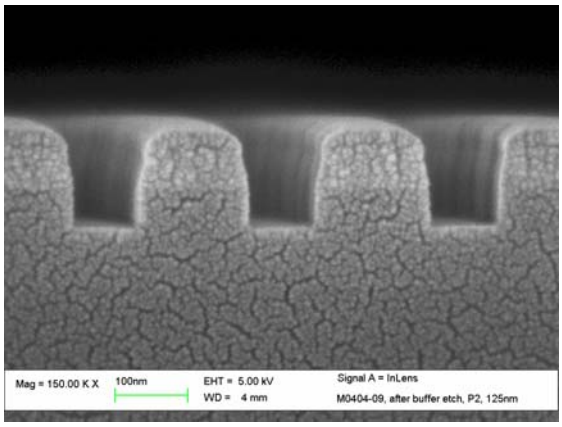

Fig. 7: P3, 125nm dense lines after absorber and buffer etching

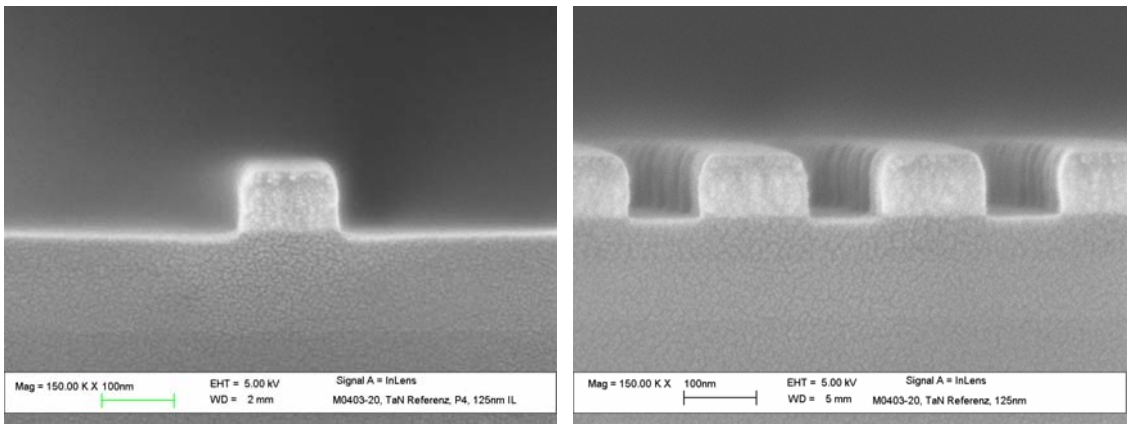

Fig. 8: 125nm isolated line/dense lines after absorber etching (reference)

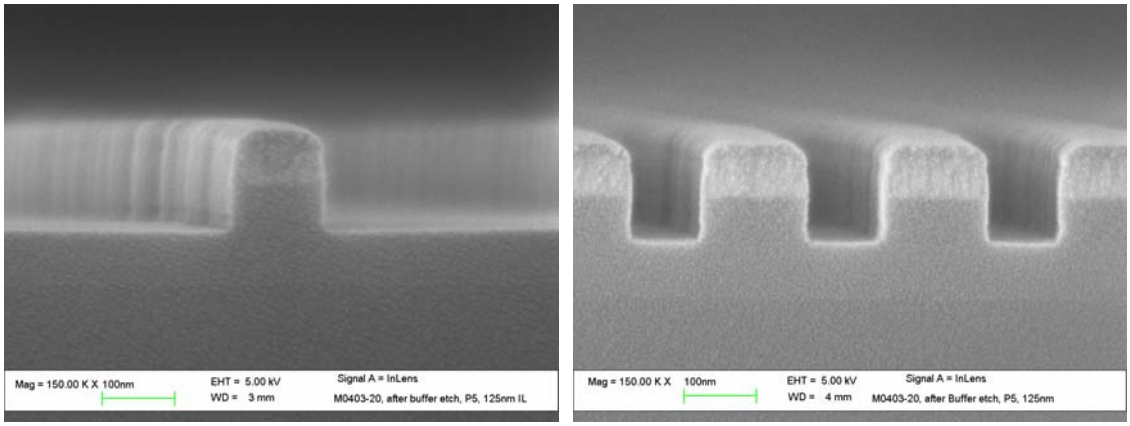

Fig. 9: P5, 125nm isolated line/dense lines after absorber and buffer etching

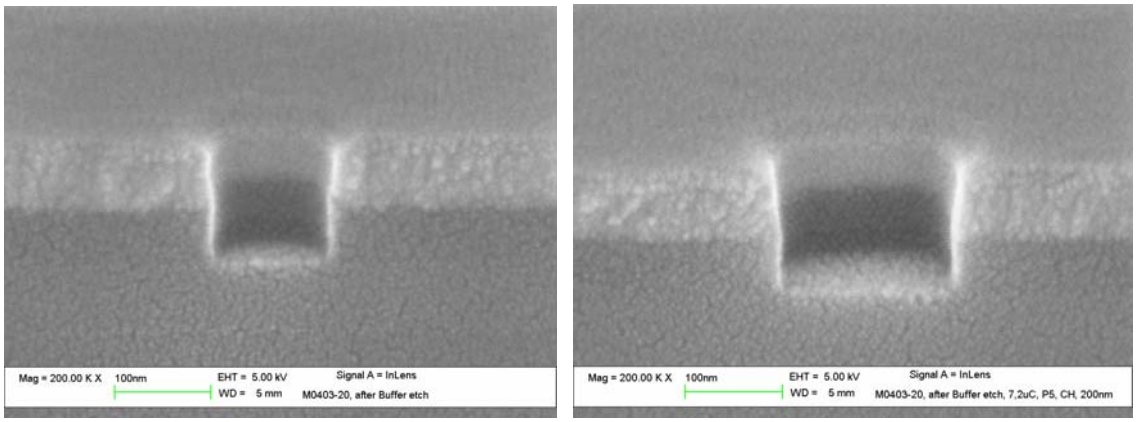

Fig. 10: P5, 125nm and 200nm contacthole after absorber and buffer etching

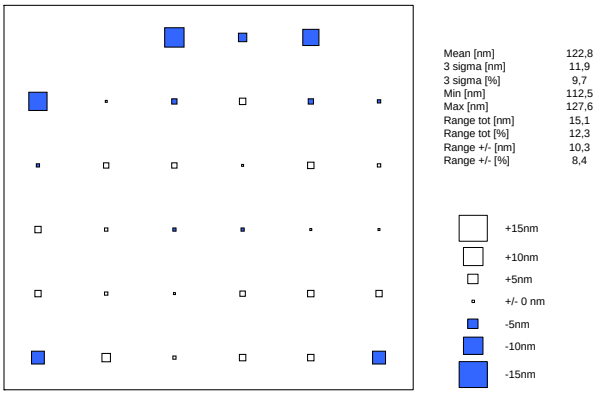

Fig. 11: CD uniformity, 150nm L&S after absorber etching

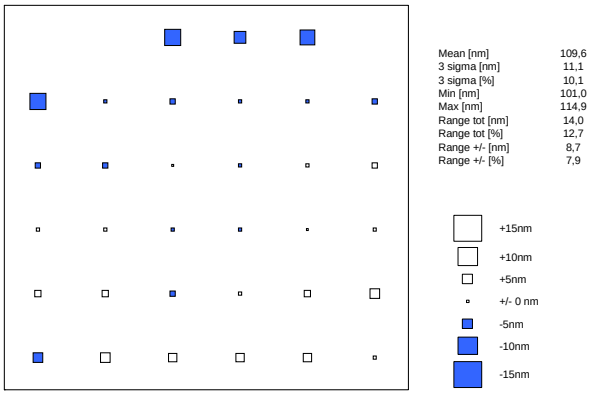

Fig. 12: CD uniformity, 150nm L&S after buffer etching

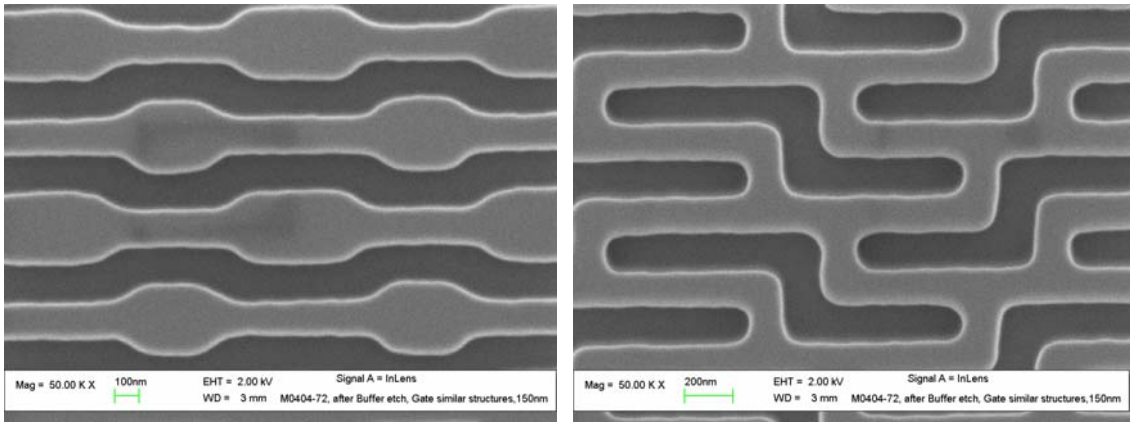

Fig. 13: 150nm poly gate similar structures after absorber and buffer etching

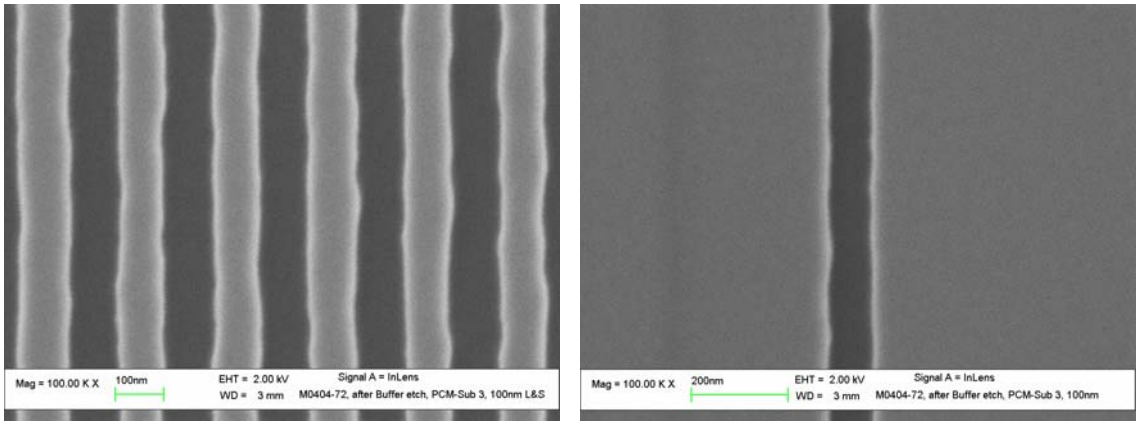

Fig. 14: 100nm dense lines/isolated space after absorber and buffer etching

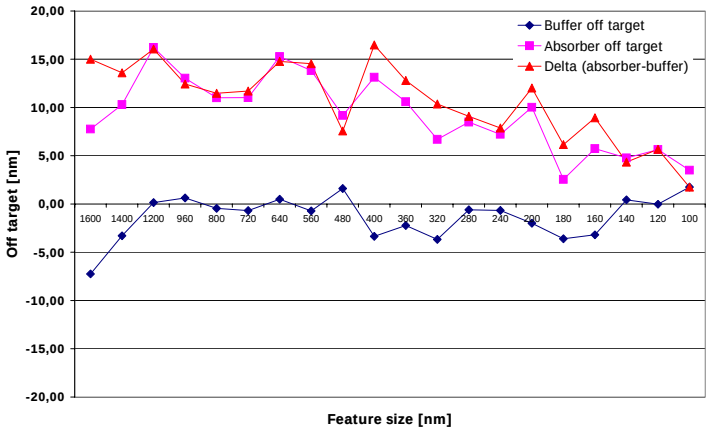

Fig. 15: CD off target, dense lines after absorber and buffer etching

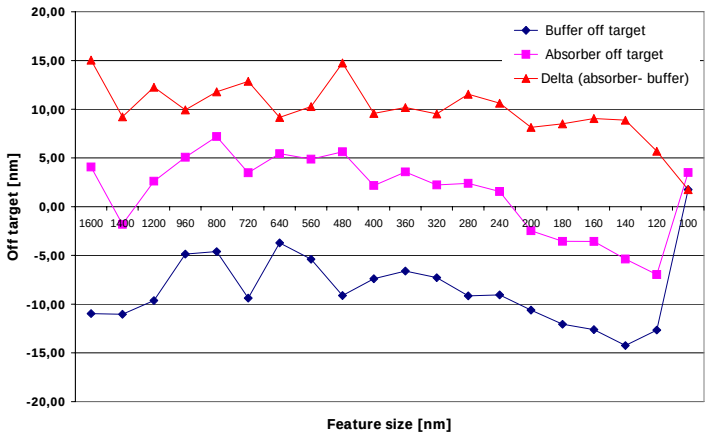

Fig. 16: CD off target, isolated space after absorber and buffer etching