Mask Data Volume – Historical Perspective and Future Requirements♫

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Abstract

Mask data file sizes are increasing as we move from technology generation to generation. The historical 30% linear shrink every 2-3 years that has been called Moore's Law, has driven a doubling of the transistor budget and hence feature count. The transition from steppers to step-and-scan tools has increased the area of the mask that needs to be patterned. At the 130nm node and below, Optical Proximity Correction (OPC) has become prevalent, and the edge fragmentation required to implement OPC leads to an increase in the number of polygons required to define the layout. Furthermore, Resolution Enhancement Techniques (RETs) such as Sub-Resolution Assist Features (SRAFs) or tri-tone Phase Shift Masks (PSM) require additional features to be defined on the mask which do not resolve on the wafer, further increasing masks volumes. In this paper we review historical data on mask file sizes for microprocessor, DRAM and Flash memory designs. We consider the consequences of this increase in file size on Mask Data Prep (MDP) activities, both within the Integrated Device Manufacturer (IDM) and Mask Shop, namely: computer resources, storage and networks (for file transfer). The impact of larger file sizes on mask writing times is also reviewed. Finally we consider, based on the trends that have been observed over the last 5 technology nodes, what will be required to maintain reasonable MDP and mask manufacturing cycle times.

Key Words: Optical Proximity Correction (OPC), Mask Data Prep (MDP), Variable Shaped Beam (VSB)

1.0 Introduction

Optical lithography continues to be used for leading-edge IC mass-production. Table 1 shows a typical feature size roadmap for microprocessor technology. With the development of immersion lithography, and the anticipated development of higher-index fluids, it is expected that the 32nm node will be achieved using 193nm lithography. To mitigate the small Depth of Focus (DOF) implied by the larger Numerical Apertures (NAs), RETs such as Off Axis Illumination (OAI), SRAFs and PSMs have been employed. In addition to advances in stepper and resist design, we have steadily reduced the k_1 factor moving closer and closer to the theoretical limit of 0.25. To correct for the increasingly large systematic biases inherent in a low-k_1 process, OPC is required. Initially, OPC amounted to a few simple rules to correct biases between 1-D features. These could take the form of either Rule Based OPC or Table Based OPC. As feature sizes decrease and 2-D patterns require corrections, the OPC rules became increasingly complex. Around the 130-90nm technology nodes a switch was made to model-based OPC[1], where a calibrated process model is used to determine the ideal edge movement required to print the original design target.

Year of Production	Technology Node	Wavelength	NA	Field Size (mm x mm)	k_1*	OPC
1998	250	248	0.57	22 x 22	0.72	Target Sizing
2000	180	248	0.7	22 x 22	0.64	Rule Based
2002	130	248	0.8	22 x 22 26 x 33	0.52	Rule & Model based
2004	90	193	0.75	26 x33	0.44	Model based
2006	65	193	0.93	26 x 33	0.39	Model based
2008	45	193	1.2	26 x 33	0.35	Model based
2010	32	193	1.5	26 x 33	0.31	Model based

Table 1: Technology Roadmap for Optical Lithography for Microprocessors
* k_1 (logic) is defined for the half pitch of the metal 1 layer, i.e. 1.25*node*(NA/λ)

The pervasive use of OPC has lead to a dramatic increase in the complexity of the MDP process. The MDP resources have transformed from single-workstations to high-performance computing clusters. 64-bit operating systems are required to handle the multi-GB file sizes created. Large disk arrays are required to store the data and fibre-optic data networks are needed to provide adequate file transfer rates. The ITRS[2] has started to include mask file sizes (defined as "The maximum file size for uncompressed data for a single layer as presented to a raster tool") as part of their roadmap. In this paper we present actual file sizes from AMD microprocessor and Flash designs as well as Infineon DRAM designs to evaluate whether the ITRS predictions are accurate.

MDP complexity in the IDM primarily concerns computer resources. In the mask shop, in addition to data manipulation, these files sizes have significant impact on tool throughput, productivity and ultimately on mask cost. Mask patterning for critical layers for 130nm technologies and below has shifted from Raster scan to high-keV Variable Shaped Beam (VSB) tools. For any particular tool, the write time is somewhat proportional to the number of shots (rectangular or triangular) that need to be exposed. An accurate prediction of the shot count is crucial for development of new VSB e-beam tools that will deliver reasonable write times at an affordable cost.

2.0 Mask Data Preparation

2.1 Increase in shot count due to OPC

To make MB-OPC accurate it is important to create sufficient edge fragments to allow for proper correction. Fragments are typically created near corners and line ends (intra-feature) and at locations where there are nearby adjacent features (inter-feature). As the k_1-factor decreases, more patterns fall within the optical interaction radius of the lithography system (~λ/NA) and consequently the amount of fragmentation increases.

Table 2 shows the shot count multiplier (for a JEOL pattern generator) i.e., the ratio between drawn and post-OPC layout, for some different layers in a Microprocessor and DRAM technologies at the 90nm node. In the case of the DRAM data, the estimate of the multiplier is based on CFLT data. It is interesting to note that for production layers, the OPC multipliers for both DRAM and Logic lie in the range 1-2.2.

	90nm Logic	90nm Logic Aggressive	90nm DRAM*
Active	1.7	14.2	2.2
Poly	1.7	7.5	2
CT	1	5.8	1.1
Metal	2.2	4.7	1.4

Table 2: OPC Shot Count Multipliers
* Shot count multiplier based on CFLT data

As an exercise to see how large the OPC shot count multipliers might become in future technologies, we performed aggressive fragmentation on the 90nm microprocessor layouts by setting the maximum fragment length to be ~30nm. This is denser than the "Nyquist Limit" ($\lambda/4(1+\sigma)$NA for partially coherent imaging) so hopefully represents an upper limit to the OPC multiplier for the edge-based OPC approaches currently employed. There is still considerable room for OPC complexity to increase – in the aggressive case, the shot-count-increase ranges from 4.5x to 14x the drawn data. Figure 1 shows examples of the drawn, standard OPC and aggressive OPC layout for 90nm metal 1 designs.

We have also looked at the impact of tiling and SRAFs. In dense layouts such as Active, Poly and Metal1 the opportunity to place tiling and SRAFs is fairly limited and so there tend to be much fewer of these figures than the drawn data. Since tiles and SRAFs typically do not get OPC we find that the impact on the file size is not significant. For contacts the difference in the file size is significant (since each contact may acquire one or more SRAFs), but since the initial figure count is lower this is still manageable.

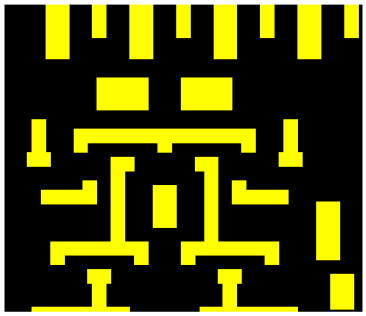


Figure 1a: Drawn Metal 1

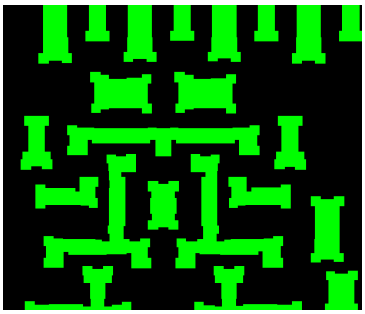


Figure 1b: Standard OPC

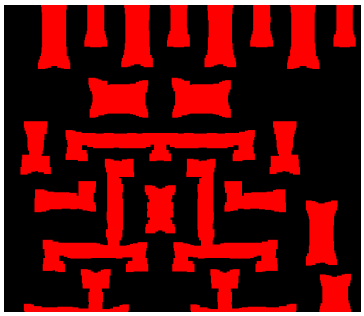


Figure 1c: Aggressive OPC

2.2 Comparison of historical shot count and CFLAT data

Increase in OPC complexity is of course only one contributor to the increase in the data file size that is transferred to the mask shop. Decreasing feature size produces significantly more complex designs as is seen in current generation multi-core microprocessors and Gigabit DRAM chips. An additional factor is the increased stepper field size that increases the number of chips per reticle that need to be written on the reticle.

To study the increase in file size presented to the mask shop, we have collected file size data for microprocessor, DRAM and Flash Memory designs from the 250nm generation down to the 65nm generation. Unfortunately we do not have shot count data for all of the data, so to make a consistent comparison we will use the CLFT file size as a constant metric. CFLT is a pattern file format most commonly used to transfer mask data to the mask shop. Our own studies (not published) indicate that, for microprocessors, the CFLT file size correlates to the shot count reasonably well. Figure 2a shows the uncompressed CFLT file size for individual product die per node. This data is representative of the file sized transferred between the customer and the mask shop. The data at each node is a combination of different critical layers and different products. The SIA roadmap maximum single layer CFLT file size is shown for comparison. It is clear that none of the individual files is near to the ITRS prediction.

All the files in figure 2a are for multi-die reticles, to calculate the worst case single die reticle we multiplied the file sizes in figure 2a by the number of dice and scaled to the largest exposure field available. This represents the size of the file that will be presented to the pattern generator. The results of this calculation are shown in figure 2b. By this metric we see that although the ITRS estimate was much too large for 250nm technology node that by the 90nm node the Full Field data size is close to the ITRS maximum file estimate (We expect the 65nm data to get much closer to the ITRS prediction as more designs are released). The rate of file increase for actual data is faster than predicted by the ITRS, implying a crossover around the 45nm

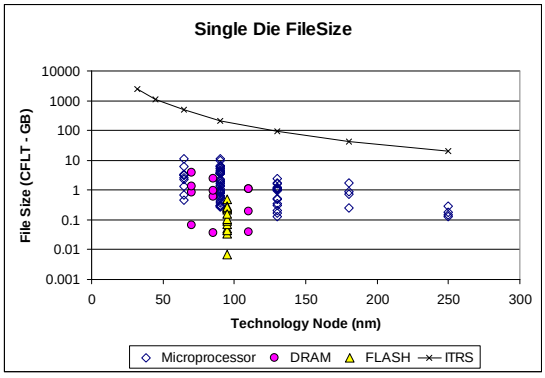


Figure 2a: Individual file size by node

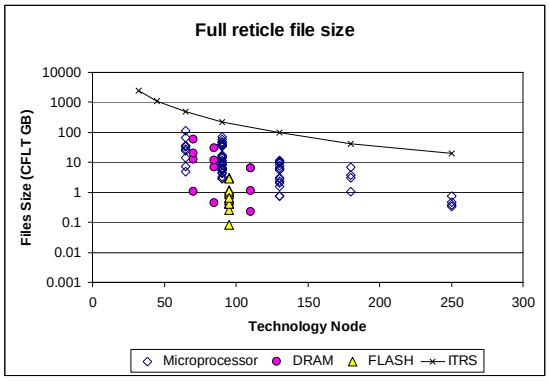


Figure 2b: Full field file size by node

2.3 MDP Runtimes

2.3.1 OPC Runtimes

The complexity of the OPC calculations creates significant computational demands. The charts below (Fig. 3a and Fig. 3b) demonstrate the trend for both the real time and cpu time for two key layers across five microprocessor technology generations. The 90nm OPC calculations were the first to require multi-threaded processing. As the scope of 65nm OPC was comprehended, it became clear that more cpus needed to be deployed and required a migration from multi-threaded applications to a distributed system. It is not uncommon to use from 100 to 200 nodes/cpus for a critical layer 65nm OPC calculations. Because of the availability of affordable high performance 64-bit x86 systems, such as AMD Opteron™, the cost of this large increase in compute time has been negligible. Going forward it is anticipated that similar cost reductions can not be achieved if 20-fold increases in computation power are required. Consequently, strong efforts have to be made to manage OPC run time by managing OPC complexity and though OPC algorithm enhancements.

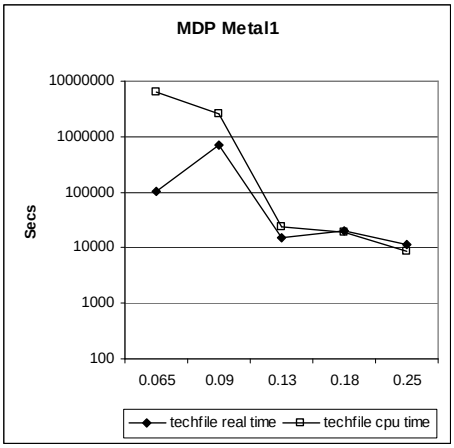


Figure 3a: OPC Run Time, Metal1

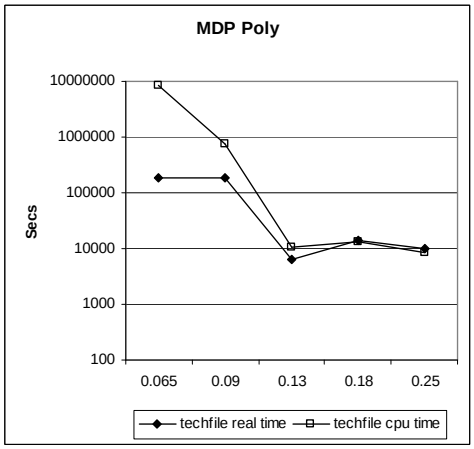


Figure 3b: OPC Run Time, Poly

2.3.2 File Transfer from IDM to Mask Shop

The conclusion of section 2.2 is that if we follow the current trend, a 1 TB full-field *uncompressed* CFLAT[3] file is likely at the 45nm node and that individual chip sizes of >100GB will be seen. There are several compression techniques that can reduce the data volume: from generic gzip to application specific compression to hierarchical forms of data , such as CREF[3]. Each of these options has to be examined to determine which offers the best ROI as each has trade-offs in cost and data prep cycle time. A distinct possibility that is beginning to be utilized is the new OASIS[3] format for stream data. A likely flow would utilize OASIS data as the format to hand-off to the mask shop. With typical reductions in file size of 10-30x (for GDS data), it appears that an OASIS-based flow would prevent data file size issues from being a significant problem for another 2 technology nodes. This flow, however, requires a migration from a fracture format data, like CFLAT, to a polygon based-data format.

With these large data sets, the transfer to the mask shop has become challenging. Dedicated T1 links have been the standard for secure reliable transfers utilizing simple FTP. The increase in data volume as well as the sporadic nature of mask data transfers means that the use of dedicated, high-bandwidth circuits is costly and ineffective. The current trend is to use dedicated VPN tunnels over existing public circuits to achieve acceptable performance. Throughput for these configurations is reasonable using single threaded transfers, while maximum performance can be achieved using multi-threaded transfers. In regards to internal transfers, there is obviously a need for high bandwidth, low latency connectivity for effective collaboration in global companies. Despite the caveats mentioned, we are confident that data volumes and file transfer will remain manageable problems for the next 2 technology nodes.

2.3.3 Mask Shop Data Prep Issues

Typically, most mask shops do not perform OPC, however the number of data manipulations performed in the mask shop is increasing. Traditional activities such as tone reversal, biasing and conversion to the correct pattern generator format are all impacted by the increasing post-OPC file size. Newer activities, such as Mask Manufacturability Rule Checks (MRCs)[4] are also driving increasing computation requirements in the mask shop Luckily, while Moore's Law drives the increase in data complexity it also makes possible faster computers at lower cost. Even with the introduction of distributed parallel processing schemes, the hardware cost to maintain a constant 4-hour cycle time has decreased as shown in figure 4a. Unfortunately the same cannot be said for MDP software costs, which, while constant or declining up to 2002 have begun to climb significantly as shown in figure 4b.

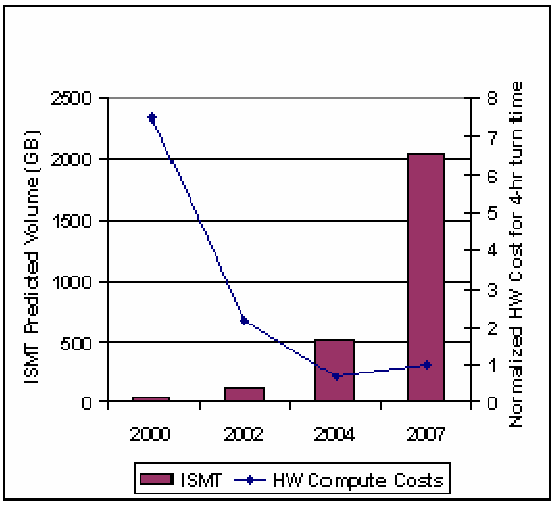


Figure 4a: Mask Shop Hardware Costs

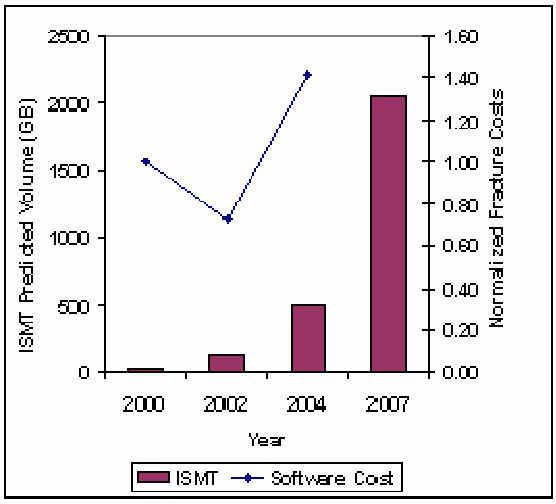
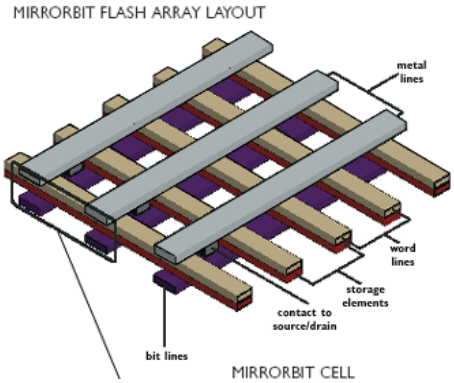


Figure 4b: Mask Shop Software Costs

2.4 Comments on Microprocessor vs Memory designs

[Comment: I would really like to have the shot count data for DRAM here so we can say with confidence whether the CFLAT data is preserving hierarchy and whether the comparison of CFLAT data between Logic and Memory predicts the shot count.]

The data presented in this paper from Microprocessor designs is probably a reasonable predictor for other logic designs such as ASICs, GPUs, Chipsets and even FPGAs. DRAM and FLASH memory have also been included. Looking at the post-OPC file sizes for DRAM and FLASH files, we find that in both cases the CFLAT file size and shot counts are significantly smaller than for logic parts made at the same technology node. (despite the fact that the minimum pitch for 90nm DRAM is ~180nm, versus 240nm -280nm for 90nm Logic. The post-OPC (CFLT) data for memory designs is smaller than microprocessor designs because they have very hierarchical layout, and a significant amount of the hierarchy is maintained after OPC. The shot count, however, represents fully flattened data. There are a couple of factors specific to memory designs which keep the shot count acceptable: i) the layout of the DRAM[5] and FLASH bitcells comprises mostly of long straight lines (figures 5a and b), as such the OPC multiplier for the core is ~1 and ii) with a maximum shot size of ~ $1\mu m^2$ it is possible to define multiple bitcell elements with a single exposure shot.



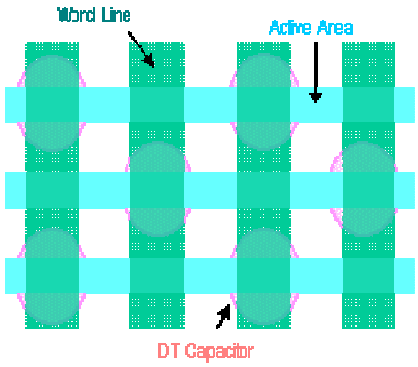


Figure 5a (FLASH Bitcell)

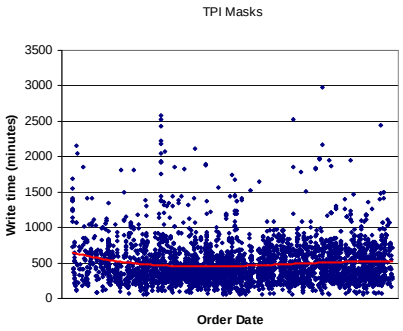
Figure 5b (DRAM bitcell)

3.0 Impact of file size on write time

3.1 Historical Write time data

Prior to the 130nm node, AMD used laser pattern generators exclusively for mask writing. These tools use a raster-beam strategy and address every pixel on the mask during the write process. As a consequence, unless the data is very dense and the data transfer rate internal to the write tool becomes the rate limiting step, the write times for these tools are tightly distributed around a typical, 120 minute, write time.

Beginning at the 130nm node AMD adopted a strategy of using both VSB e-beam and laser pattern generators. Write times for VSB masks written by AMD (microprocessor layouts) and Toppan Photomasks Inc. (many kinds of layouts including DRAM and Logic) over a 5 year period are shown in figure 5a and 5b. We notice that in both cases the average write time has remained remarkably constant over time. The median value for Toppan Photomasks Inc. is somewhat higher than for AMD (500 vs 400 minutes). The percentage of masks with write times > 1000 minutes is 5% and 2% respectively.



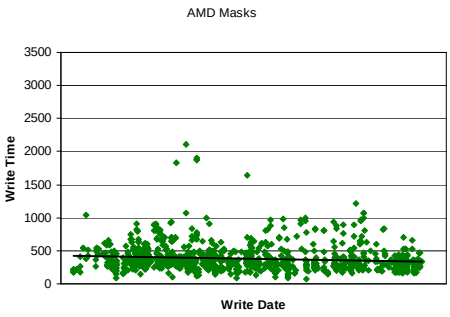


Figure 5a: Toppan Photomask Write Times

Figure 5b: AMD Write Times

3.2 Variable Shaped Beam (VSB) Writers

All leading edge masks are made on Variable Shaped Beam (VSB) e-beam writers. There are two main writing strategies.

1) Stepping Stage: In this arrangement, the pattern is divided into square fields. The patterns within each field are composed of a multitude of rectangular (or in some cases 45° triangular) shots. The stage is stepped from field to field and the beam is deflected within each field to expose each shot serially.
2) Scanning Stage: In this arrangement, the pattern is divided into rectangular stripes. The patterns within each field are composed of a multitude of rectangular (or in some cases 45° triangular) shots. Stage scans each stripe and retraces, the shots are exposed “on the fly”. Stage speed is determined by local shot density

Complex write time estimation models can be made for these two writing strategies. For the stepping stage approach it is necessary to know the stage move and settle time, field size and pattern extents to calculate the time to step across the full extent of the reticle. Within each field it is necessary to know the number of shots, the time to expose each shot and the deflector settle time and other overheads. For the scanning stage, the shot exposure time, based on beam intensity and resists sensitivity, and local shot density determine stage speed. Knowing the scan height, pattern extents and stage retrace time, the write time can be calculated.

If estimating the write time to within 25% accuracy is sufficient, however, it appears that a simple linear model may be sufficient. Figure 6 shows linear fits to the write time versus shot count data for two generations of VSB tool (from 2 different manufacturers).Particularly for patterns of equal extents, shot count is a reasonably accurate predictor of relative write time.

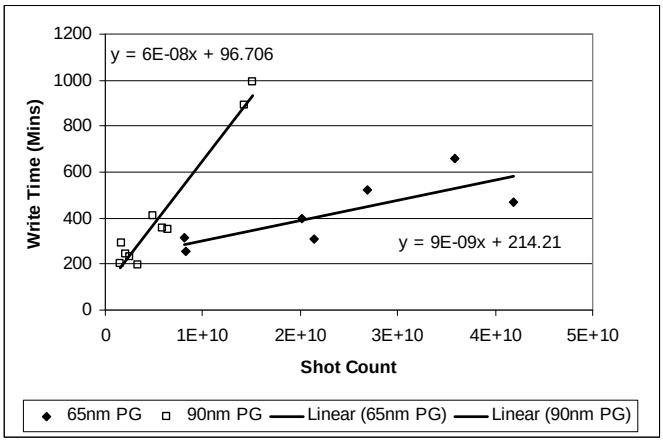


Figure 6: Write Time as a function of Shot Count

4.0 Discussion

4.1 Expected OPC multipliers

We consider two different approaches to calculate the expected shot count density for future technology nodes (using only microprocessor data). In the first method to estimate the OPC multiplier we consider the CFLAT density per μm^2. Figure 7 shows the data from figures 2a and 2b re-plotted in this manner. Based on the fit to the data we predict ~2.15x increase in feature density per generation (versus 2x implied by Moore's law).

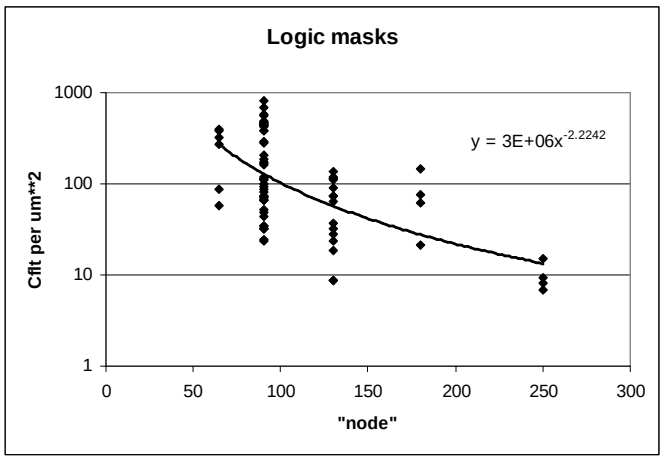


Figure 7. Pattern (Cflt) Density Trend

A second estimate of OPC multiplier can be made using the data in table 1. Simple scaling tells us that the figure count will increase as $(\text{pitch})^{-2}$. The OPC interaction radius (i.e. the distance over which a particular geometry may influence, optically, another) is proportional to k_1^{-2}. Combining the feature size and k_1 data in table 1 we calculate a shot count multiplication trend shown in figure 8. Based on this data a 2.5x increase in overall figure count per generation is expected.

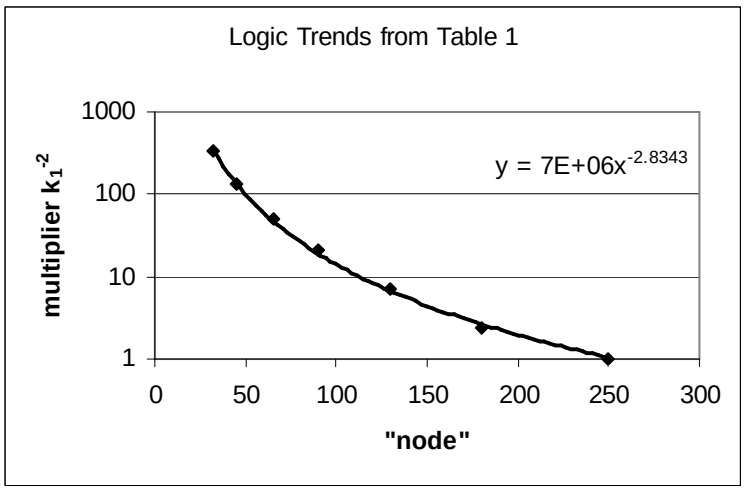


Figure 8: Estimated Figure Count Multiplier from Table 1.

4.2 Expected shot counts

Since the field size for scanners is limited by the choices of 4x magnification and 6" reticle substrates to 26mmx 33mm on the wafer we do not anticipate any increase in the reticle written are to occur at the 45 or 32nm nodes. Furthermore, we do not anticipate any radical change in the model based OPC approaches. i.e. although the fragmentation may increase modestly from node to node we do not expect a change to pixel based masks. Extrapolating current trends indicates that Nyquist sampling will be achieved for some levels by the 32nm node. Consequently, a worst case scenario would predict figure counts per node to increase by a factor of ~2.15 - 2.5, based on the analysis in section 4.1 (versus the doubling implied by Moore's law).

4.3 Anticipated write tool improvements

Will e-beam writers be able to keep up with the increase in shot count? Current data shows that in general the VSB tools have done a good job of improving performance to keep the average write time a constant (see figures 5a and 5b).

To explore the potential of VSB tools to accommodate the expected increase in shot count from node to node we generated a simple write time model for a stepped stage VSB tool similar to the JEOL 9000MVII and 3030MV tools currently in use at Toppan Photomasks. Three components of write time are considered – shot exposure time (resist exposure), stage movement time (positioning the stage under the electron beam column, and shot overhead (deflection electronics stability time constant). Shot exposure time is simply the resist dose expressed C/cm^2 divided by the beam current density (A/cm^2) multiplied by the shot count. Stage movement time is equal to the area of the mask pattern divided by the area of a field multiplied by the number of stage passes. Beam overhead is the summation of several overhead constants multiplied by the shot count and by the number of passes. The write conditions for a hypothetical 90-nm µP metal-1 layer were used as a baseline to study the impact of increasing shot count from node to node. With a pattern area equal to the size of a scanner field (104 x 132 mm at mask scale) and a shot count of 15 billion shots the total predicted write time on a JEOL-9000 is 14.3 hours of which 19% is stage movement time, 52% is shot exposure time, and 29% is shot overhead. Given the limitations on increasing the exposure area based on scanner field size, the primary change from node to node will be an increase in shot count. Figure 9 illustrates the projected increase in write time, *assuming only a 2x increase in shot count per technology node*. Stage motion time remains constant since the pattern extents haven't changed. Shot exposure time and shot overhead increase linearly with shot count. From this example it becomes clear that reducing the shot time and shot overhead are key to maintaining throughput as shot count increases.

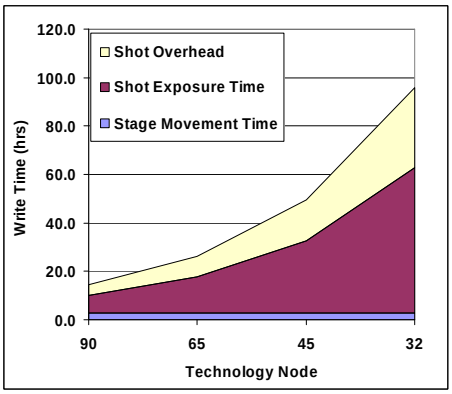


Figure 9: VSB Write Time Budget

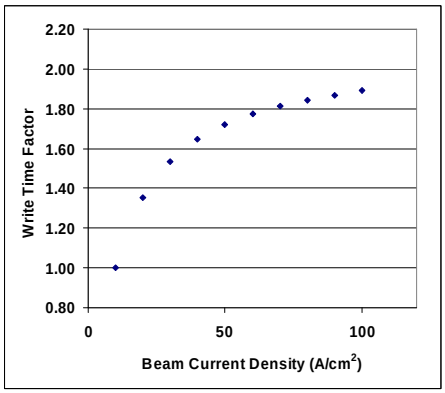


Figure 10: Impact of beam current

To reduce exposure time it is necessary to either reduce the dose required to expose the resist (increase resist sensitivity) or increase the current density of the beam. Increasing the resist sensitivity might be possible, but there are no known solutions at this time. In addition, shot noise has been suggested as a fundamental limitation of sensitivity that may reduce the value of higher sensitivity resists[6]. Increasing current density is possible and current generation VSB tools employ up to 50 A/cm^2 beam currents compared to earlier generations that used 10 A/cm^2. It is expected that beam current densities of up to 100 A/cm^2 may be possible although resist heating effects may limit the maximum current density possible without impacting CD performance[7,8]. The traditional method to compensate for heating effects is to increase the number of passes, thereby dividing the heating impact into multiple exposures separated by time. This increases both the stage movement time and the shot overhead time and reduces the value of lower exposure time. Figure 10 illustrates the impact of increasing beam current from 10 A/cm^2 to 100 A/cm^2 on total write time. Because shot exposure time accounts for only ~50% of the total time, increasing beam current alone only buys us about a single technology node write time. Figures 11 and 12 show similar analyses for reducing stage movement time and shot settling time, a major component of

shot overhead. Reducing stage movement from 350 ms to 50 ms only improves write time by 15-20%. Reducing shot settling time from 350 ns to 10 ns only buys us 25% improvement in write time.

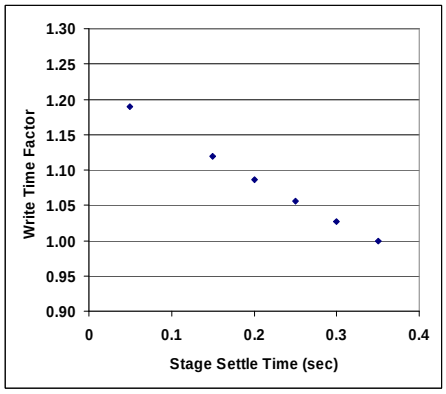


Figure 11: Impact of Stage Settle Time

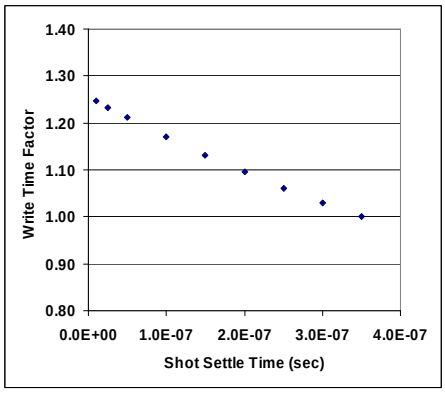


Figure 12: Impact of Shot Settle Time

What if we were able to build a hypothetical tool that incorporated all of the potential improvements discussed into one tool? Figures 13a and 13b explore this possibility. We plot the predicted write time from the 90-nm node through the 32-nm node for a 90-nm write tool, a 65-nm write tool, and the hypothetical future tool. The 90-nm tool model is similar to the JEOL 9000MVII and the 65-nm tool model is similar to the JEOL 3030MV. Note that the 65-nm tool model suggests manages to keep pace with the increase in shot count, and this is our practical experience as well. In figure 13a we shows the write times assuming only a 2x increase in shot count per technology node. In figure 13b we indicate the write times for a 2.5x increase in shot count as predicted by historical data in sections 4.1 and 4.1. The hypothetical future tool also seems to support sub-20hr write times if introduced by the 32-nm node and strong efforts are made to limit shot count increases to 2x per node (figure 13a), however if 2.5x shot count increases per node are expected then write time will be nearer 40hr. Remember that this tool may require measures to reduce resist heating effects. Methods that use multiple passes will reduce the throughput by on the order of an additional 50% (as shown by the "Future Tool 4-pass" model in figures 13a and 13b). Other methods like shot ordering may adversely affect throughput[9].

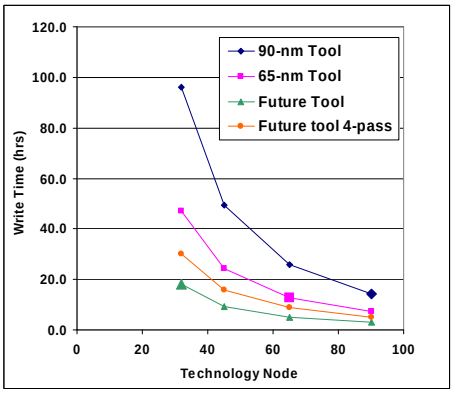
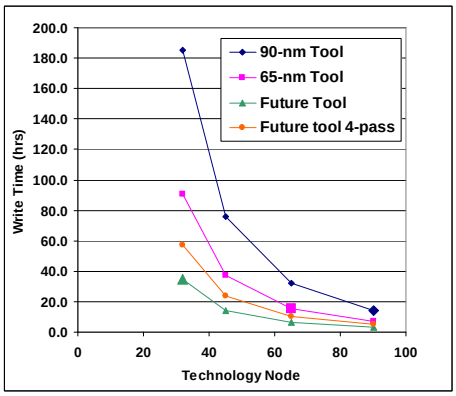


Figure 13a: Prediction (2x per generation)



13b: Prediction (2.5x per generation)

4.4 Inverse Image Masks **[Comment – Should we remove this section?]**

Our prediction is that there will not be any major change in the way OPC is performed down to the 32nm node. However, in pursuit of the optimum image many creative schemes are being proposed. One of particular interest to the mask maker is the inverse imaging mask. Proposed many years ago by Wang and Pati[10] the

concept is to consider the mask as a continuous phase/transmission object, find the best mask solution that optimized edge placement and image contrast metrics and then discretize the final object to a limited number of phases and transmissions. An example of such a mask (along with the original design) is shown in figures 14 a and b below. In this case (particularly because of the use of arbitrarily angled lines to define the patterns) the OPC multiplier is ~ 500! Simplification of this mask is possible. As a practical guideline, if the final shot count can be less than that for a metal 1 mask then it will be possible to write the mask based on our data that means that the figure count multiplier for the contact hole level must be 5-6, about 100x less than the current design. (Inspection of the final mask is another issue that we cannot consider in this paper).

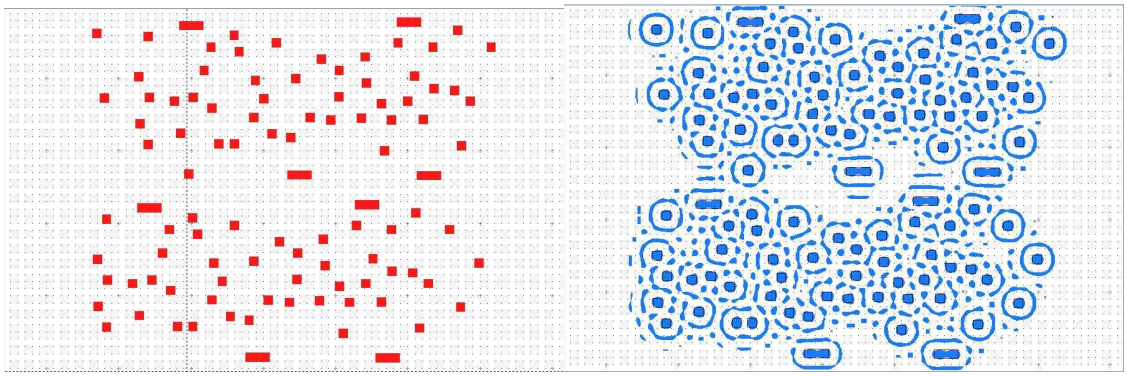


Figure 14a: Original Design

Figure 14b: Inverse Image Mask

5.0 Conclusions

We have studied the historic trends of file size for mask data. We have presented data from leading edge microprocessor and memory designs and observe that the data-processing issues and mask shot counts are primarily driven by random logic designs with model-based OPC. We have seen that despite the introduction of OPC and RETs which result in additional (non-printing) mask geometries, shot counts have increased more slowly than we had expected; by only ~2.5x per node (Moore's Law alone would predict 2x). Additionally, no "step function" in data volumes for microprocessors was seen over the 5 technology nodes studied. Although the computational and data storage resources required to support this have gone up significantly, the increase in semiconductor component and system performance enabled by Moore's law has supported this and even lead to lower hardware costs, although the same cannot be said of software costs.

When considering the progress in write time of VSB e-beam tools we observe that the write time for critical plates has remained remarkably constant over the last 5 years. We speculate, based on reasonable estimates of beam current and beam settle time improvements that masks for the 32nm node may still be written on single beam VSB tools. However, for this to occur it will be necessary for OPC engineers to be more aware of the shot count of their OPC layout as any significant deviation from a 2x per generation shot count increase will lead to significant increases in write time. Novel RETs are still being proposed, but however the final output may look, it is not possible for these masks to significantly exceed the shot count of today's masks with the current VSB tools. Consequently there will be a premium on innovative schemes to simplify such designs without sacrificing performance. Finally we would like to recommend that shot count data be more widely available, both as an estimate generated when the OPC run is completed and as feedback from the mask shop when the actual mask has been written.

6.0 Acknowledgements

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♫ This paper is largely derived from a previous paper "Mask Data Volume – Explosion or Damp Squib?" Presented at the 2005 BACUS Photomask Symposium (SPIE vol. 5922 in press). The major changes in this paper are the inclusion of DRAM and FLASH memory data and some changes of wording for clarification and to make the conclusions clearer.

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