EUV lithography is the prime candidate for the next generation lithography technology after 193 nm immersion lithography. The commercial onset for this technology is expected for the 45 nm half-pitch technology or below. Several European and national projects and quite a large number of companies and research institutions in Europe work on various aspects of the technological challenges to make EUV a commercially viable technology in the not so far future. Here the development of EUV sources, the development of an EUV exposure tools, metrology tools dedicated for characterization of mask, the production of EUV mask blanks and the mask structuring itself are the key areas in which major activities can be found. In this talk we will primarily focus on those activities, which are related to establish an EUV mask supply chain with all its ingredients from substrate production, polishing, deposition of EUV layers, blank characterization, mask patterning process and the consecutive metrology and defect inspection as well as shipping and handling from blank supply to usage in the wafer fab. The EUV mask related projects on the national level are primarily supported by the French Ministry of Economics and Finance (MinEFi) and the German Ministry of Education and Research (BMBF).

Keywords: EUV, mask substrate, mask blank, mask patterning, CD metrology, inspection, handling, supply chain

1. INTRODUCTION

During the past 3 years the MEDEA+ EXTUMASK project worked on establishing a production infrastructure for experimental EUV masks down to the 45 nm half-pitch node. A search for new materials had to be conducted and manufacturing solutions be found in order to achieve the required physical parameters concerning flatness, reflectivity and foremost low defect density. Once a blank material exists the structuring processes need to be developed, that will transform the blank material into fully functioning mask for lithographic purposes. Here the main requirements are to achieve the desired structure sizes (called critical dimensions – CD) with a high degree of uniformity (CDU) across the complete plate. During processing the optical and physical properties of the blank material need to be preserved and verified. Tools, which are capable of measuring dimensions and positions in the regime up to the required precision were not existing at the beginning of the project or were not adequately suited to work with these new materials of the EUV masks. Defects created by the processing and handling of the plate(6,10),(994,993) need to be detected and subsequently be removed before the plate is shipped to the customer. During the shipment and handling time in the wafer fab the defect and particle free masks have to be kept clean. Current handling technology is not sufficient for the pellicle-less EUV plates. The EXTUMASK project has covered all these aspects of the mask production and handling chain and has achieved a considerable progress not only in the understanding of the underlying problems but has provided solutions in these areas or at least a clear path for the solutions of the problems. The European “More Moore” project continues these activities for the 32 and 22 nm half pitch node. Focus for the EUV mask sector within the project is on the feasibility of processes for the smaller nodes and on handling of EUV reticles in the wafer fab.

2. STEPS TOWARDS A MASK PRODUCTION INFRASTRUCTURE

1.1. Mask Substrates Production

The main challenge for the mask in the EUV regime is that a new material combination has to be found that allows to image pattern on the mask with a high precision in reflective mode. This reflectivity is created by a multi-layer mirror
using 40 or more bi-layers of Molybdenum (Mo) and Silicon (Si). Since the reflectivity of this multi-layer mirror is theoretically limited to about 70% for a wavelength of 13.5 nm at about 6 degree angle of incidence, the rest of the light is absorbed in the mask material. This creates the demand for a low thermal expansion material (LTEM) as a substrate for the mask. The expansion coefficient of the material for production purposes needs to be well below 10 ppb/K (specification value is 0 ± 5 ppb/K). Further requirements on this LTEM substrate are the required flatness and thickness limits of below 50 nm peak-to-valley to prevent in-plane distortions of the patterns exceeding the limits for the respective nodes under the conditions of a full field chucked reticle. Roughness requirements as well as defect levels of the substrate surface pose additional challenges for their production.

Figure 1 Typical shape of a polished LTEM substrate front side in the quality area. The sample shown was taken out of a commercial substrate polishing process.

The focus of the mask substrate production therefore has been laid on the supply of flat substrates with a low defect rate. Materials that have been studied include ULE, Clearceram, Zerodur and a new glass ceramics developed by SCHOTT AG. Polishing techniques have been developed by SAGEM, SESO, and SCHOTT Lithotec that will allow to reach the required flatness of the low thermal expansion substrate materials. The main focus of the partners is to not only show the availability of the technological process itself but also to look for a commercial viable solution. Polishing techniques originally developed for fused-silica glass were successfully transferred to LTEM substrates. During the last few years a multi stage process approach was followed that starts with a collective polishing of several substrates in one go and than proceed with single plates. Intermediate cleaning steps will be applied. Depending on the required flatness the next step will either proceed with a final collective finish polishing or with special correction methods like e.g. ion beam figuring or magnetorheology. Figure 1 shows the results of a standard flattening/polishing techniques provided by SCHOTT Lithotec. The final clean will remove the majority of particles created by this process. Parameters achieved in this process can be seen in the table below.

<table>
<thead>
<tr>
<th>Specification SEMI-P37</th>
<th>Actual values reached</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Expansion Coefficient</td>
<td>0 ± 5 to ± 30 ppb/K to 0-10 ppb/K ± 10 ppb/K</td>
</tr>
<tr>
<td>Useful area</td>
<td>142 x 142 mm (centered on each side)</td>
</tr>
<tr>
<td>Flatness</td>
<td>50 nm (rear and front surfaces) 50 – 150 nm</td>
</tr>
<tr>
<td>Roughness front surface</td>
<td>&lt; 0.15 nm RMS period of analysis &lt; 10 µm 0.10 – 0.30 nm</td>
</tr>
<tr>
<td>Defects</td>
<td>0 &gt; 32 nm 0.007 def/cm² &gt; 200 nm 0.02 def/cm² &gt; 150 nm</td>
</tr>
</tbody>
</table>

Table 1 Selected substrate performance data in comparison to the SEMI-P37 specification values.

The progress made in this area during the project is quite impressive. LTEM materials can now be produced under commercial conditions reaching the best classes for the expansion coefficient. While at the beginning of the project no substrate material existed with a flatness of less than 500 nm, single sided flatness has now reached the 50 nm, which is the target for the EUV regime. Defect levels have gone down from 600 def/cm² (@200 nm cut-off size) to a level of 0.007 def/cm² , which is a remarkable progress and already quite close to the final required values for this cut-off value. The remaining progress needed is to improve the defect measurement sensitivity down below 50 nm and to reach the defect level and the required flatness on both sides at the same time.
1.2. Mask blank layer deposition processes

The multilayer deposition for creating the EUV reflective layer system within the specifications is the most challenging task of all. At the beginning of the project no commercial solution existed for this process. Now multilayers can be produced routinely with a reflectivity above 65%. Details of the deposition process have been looked at and mechanisms of layer intermixing in dependence of deposition process parameters and temperature treatment have been studied and its influence on reflectivity determined. Layer stress values have been found to be inversely correlated to defect levels. However, the defect level itself during deposition of the multilayers is still quite far from the necessary values. The best defect density obtained so far is 0.05 def/cm² at 150 nm cut-off size. There are strong indications that smaller particles are primarily being created by the deposition process itself while larger particles are generated due to handling. Consequently, members of the EXTUMASK consortium have developed a new ion beam deposition tool, which will address both of these issues. First layers have just been deposited with this new tool but conclusive results will require a detailed study.

![Particle-minimized ion beam sputter system Seg-IonSys-1900 built by the AIR consortium (Roth&Rau, IOM and AIS Dresden). Key elements are the linear ion beam source and the vertical reticle handler system.](image)

**Figure 2** Particle-minimized ion beam sputter system Seg-IonSys-1900 built by the AIR consortium (Roth&Rau, IOM and AIS Dresden). Key elements are the linear ion beam source and the vertical reticle handler system.

![AFM image of a 40 period MoSi multilayer studied by AIR. The rms value for the surface roughness was found to be only 0.10 nm.](image)

**Figure 3** AFM image of a 40 period MoSi multilayer studied by AIR. The rms value for the surface roughness was found to be only 0.10 nm.

The major obstacle for a fast improvement in multilayer defect levels is the absence of sufficiently sensitive defect detection tools at those companies and institutes working on multilayer deposition. The tools need to be sensitive enough for particles in the range well below 80 nm. Tools that have been developed in the framework of the project are suited for basic studies in this field but are not adequate to support the learning in a commercial environment, which can then be applied directly to the production. For faster learning some project members are using the access possibility to the tools in the mask blank development center at SEMATECH North. Within the “More Moore” project the question of
new processes for a defect free multilayer deposition technique is one the key elements to be studied in the EUV mask blank packages.

From lithographer’s point of view the prime parameters to monitor, besides the defect levels, are the reflectivity and its uniformity across the plate, as well as the uniformity of the centroid wavelength. All of this aims at the stability of the dose required to create the required structures in the wafer resist. From the mask maker’s point of view the mechanical properties, like e.g. the stress of the multilayer or the stability against influences from the environment, especially during exposure, are of equal importance. Stress in any of the layers will lead to an in-plane-distortion of the patterns created on the mask and hence a reduced performance with respect to the overlay requirements of the wafer fab.

TaN based layers were developed and choose to be the prime candidate for the absorber material because of its superior dry etch behavior with almost not etch bias. The performance of this material was found to be much better than Cr based absorbers used in standard lithography masks. The TaN based absorber was tuned in 2004 by SCHOTT Lithotec for an inspection wavelength of 257 nm which required an adaptation of the anti-reflected-coating material composition while keeping a reflectivity of below 1% in actinic light (see Figure 4). The thickness uniformity of the new layer is better than 0.7% (3sigma), while the dry etch behavior could be retained. The buffer material SiO$_2$ used within the project was reduced in height due to the successful development of a nanomachining based repair method, which will be described later in this paper.

![Figure 4](image_url)

**Figure 4** Reflectivity of the SCHOTT Lithotec TaN absorber optimized for 257 nm inspection (left) and the corresponding dry etch etch profile with a uniformity better of 9 nm and sidewall larger than 88° (right) developed by IMS Chips

### 1.3. Simulations

CEA Leti has performed extensive simulations to determine the optimal material combination for the absorber stack system and compared the optical behavior of these materials to their newly developed material denoted by $\alpha/\beta$ for the absorber/buffer stack. The goal of the study was to find a material combination with the smallest absorber stack thickness to reduce the shadowing effect during exposure. The results of these simulations can be found in Table 2.
<table>
<thead>
<tr>
<th>Absorbing stack (Absorber/Buffer)</th>
<th>Reflectivity at 13.5 nm</th>
<th>Reflectivity at 248 nm Stack: ML + Buffer Layer</th>
<th>Reflectivity at 248 nm Stack: ML + Buffer Layer + Absorber layer</th>
<th>Total thickness of the absorbing stack (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TiN/SiO$_2$</td>
<td>R&lt;1%</td>
<td>70%</td>
<td>30%</td>
<td>155 nm (&lt; D-class)</td>
</tr>
<tr>
<td>TiN/Si$_3$N$_4$</td>
<td>R&lt;1%</td>
<td>73%</td>
<td>30%</td>
<td>125 nm (&lt; D-class)</td>
</tr>
<tr>
<td>Cr/SiO$_2$</td>
<td>R&lt;1%</td>
<td>43%</td>
<td>54%</td>
<td>95 nm (&lt; D-class)</td>
</tr>
<tr>
<td>Cr/Si$_3$N$_4$</td>
<td>R&lt;1%</td>
<td>58%</td>
<td>55%</td>
<td>90 nm (&lt; D-class)</td>
</tr>
<tr>
<td>β/SiO$_2$</td>
<td>R&lt;1%</td>
<td>67%</td>
<td>35%</td>
<td>101 nm (&lt; D-class)</td>
</tr>
<tr>
<td>β/Ge</td>
<td>R&lt;1%</td>
<td>57%</td>
<td>15%</td>
<td>74 nm (C-class)</td>
</tr>
<tr>
<td>Ge/α</td>
<td>R&lt;1%</td>
<td>12%</td>
<td>10.3%</td>
<td>64 nm (B-class)</td>
</tr>
<tr>
<td>R~1%</td>
<td>11.9%</td>
<td>3.6%</td>
<td>62 nm (A-class)</td>
<td></td>
</tr>
<tr>
<td>TaN/Cr</td>
<td>R&lt;1%</td>
<td>59%</td>
<td>7%</td>
<td>90 nm (B-class)</td>
</tr>
<tr>
<td>R&lt;1%</td>
<td>59%</td>
<td>4%</td>
<td>100 nm (A-class)</td>
<td></td>
</tr>
<tr>
<td>α/Ge</td>
<td>R&lt;1%</td>
<td>57%</td>
<td>18.4%</td>
<td>70 nm (D-class)</td>
</tr>
<tr>
<td>R&lt;1%</td>
<td>14.5%</td>
<td>9.5%</td>
<td>75 nm (C-class)</td>
<td></td>
</tr>
<tr>
<td>α/SiO$_2$</td>
<td>R&lt;1%</td>
<td>50%</td>
<td>4.5%</td>
<td>82 nm (B-class)</td>
</tr>
<tr>
<td>α/β</td>
<td>R&lt;1%</td>
<td>23.2%</td>
<td>1.4%</td>
<td>91 nm (A-class)</td>
</tr>
<tr>
<td>TaN/SiO$_2$</td>
<td>R&lt;1%</td>
<td>46%</td>
<td>0.01%</td>
<td>75 nm (A-class)</td>
</tr>
<tr>
<td>α/β</td>
<td>R&lt;1%</td>
<td>2%</td>
<td></td>
<td>60 nm (A-class)</td>
</tr>
</tbody>
</table>

Table 2 EUV and DUV performances of the stack α/β compared to a large variety of bi-layer stacks. ML: Multilayer, D-class: DUV reflectivity lower than 20%, C-class: DUV reflectivity lower than 15%, B-class: DUV reflectivity lower than 10%, A-class: DUV reflectivity lower than 5%.

1.4. Mask Patterning

As a starting point for the development of the patterning the resist process has been evaluated in view of the effects of the conductive backside coating. With a standard 300nm thick positive CAR resist studies of the effects of backside coating on dose and stability have been performed. Resist structures with an aspect ratio of 3:1 where still found to be stable allowing a resolution adequate for the target nodes of EUV, the shape of resist lines is of the same quality with backside coating as compared to a non coated blank. The Figure 5 shows an example for 100 nm resist structures within different topologies.

![Figure 5](image_url)

Figure 5 100 nm resist structures on a blank without (left) and with (right) Cr backside coating

A lot of effort has been spend in 2004 to refine the patterning processes, which previously had been applied primarily to match the requirements of masks for the micro exposure tools, for full field mask applications. Two types of EUV masks have been worked on – the classical absorber binary mask type (ABM) as well as a variant that creates the pattern by etching directly into the multilayer, the so-called etched multilayer binary mask (EMBM). Dry etch processes have been developed and refined for both mask types. Due to the Cl$_2$ based etch chemistry the TaN dry etch process has virtually no etch bias $^{2,6}$. This allows the development of a process, which is capable to create line/space structures as well as contact holes at the same time and with the same quality. The current performance of the dry etch processes
allow the creation of these structures down to the dimensions required for the 45 nm and even the 32 nm technology. The pictures in Figure 6 show top-down SEM images e.g. of line/space structures created by the IMS Chips institute in Stuttgart. These structures can be created with an absorber angle of above 85° and a CD uniformity of dense structures in the range below 8 nm.

![Figure 6](image)

*Figure 6* Dense line/space and isolated space structures of an absorber binary mask (top) and contact holes (bottom) for selected structure sizes. This process was developed by IMS Chips on EUV blanks from SCHOTT Lithotec.

Much of 2004 was devoted to the integration of the unit mask processes to an integrated mask production flow. Detailed studies have been performed to match the patterning tool to the process parameter including x-y, dense-iso, and clear-dark biasing.

Besides working on the experimental development of the two describes mask types, feasibilities studies on EUV phase shifting masks have been started. These works will be continued within the More Moore project aiming at mask type evaluation for the 22 nm node and beyond.

### 1.5. CD Metrology

An essential part of the verification of the mask process quality is dedicated to the measurement of critical dimensions (CD) and their uniformity (CDU) across the plate. During the course of the EXTUMASK project Leica developed a dedicated objective for 248nm water immersion operation. The 19 single lens elements are made from fused silica and calcium fluoride. The numerical aperture of 1.2 results in a Rayleigh feature size resolution of 60 nm. The objective has been integrated into two beta metrology tools one of them has already been sold.

The majority of process development work, however, has been conducted with CD metrology based on SEM. Here the different secondary electron response of the materials used has to be properly investigated in order to understand what part of the pattern structure is actually measured. AMTC with its partner PTB has launched an extensive study to simulate the behavior of a typical absorber stack system. Parameters varied during the simulation encompass for example layer thickness, sidewall angle, corner rounding and secondary electron yield of the material in the stack. On the tool side parameters like electron energy and beam size have been incorporated. The models were compared with the measured results from a mask created with different line profile shapes. The secondary electron response curves agree quite well between the measured and simulated data (see Figure 7). It was shown that for different layer thickness in the absorber/buffer stack and the algorithm used, the CD measurement for trapezoidal shapes is sensitive to either the top or the bottom of the structure depending on the secondary electron yield of the buffer material.
Figure 7 The isolated line on the mask, as shown in the cross section, has resulted in the measured secondary electron signal in a top-down CD SEM (dotted line). The solid line is the simulated response of the material used.

1.6. Image Placement
The ITRS roadmap specifies a placement accuracy of structures on an EUV mask for the 45 nm node of 11nm. All effects contributing to this placement error have to be properly understood and minimized. One of the largest contributions for the reflective mask architecture comes from the topology of the mask surface either present from the shape of the mask blank itself or resulting from the deformation of the mask during patterning. In both cases the stress of the unpatterned and patterned layers play a dominant role. The AMTC has performed a set of detailed simulations under various conditions. These simulations are in good agreement with experiments performed at the IMS Chips \(^1\). For this a mask with registration crosses has been partially etched and the patterned placement measured after each step. If this experiment is performed with subsequent steps removing further material a precise determination of the layer stress is possible, which agrees quite well with values obtained from other methods (Figure 8). Depending on the stress of the patterned layer the displacement of structures can be quite substantial.

Figure 8 Image displacement after partial removal of the absorber layer. A very good agreement is found between experimental data (left) and the results of a finite element simulation (right)

In separate study the impact of the different clamping and chucking methods on in-plane-distortions in the patterning, registration and exposure tools has been looked at \(^1\). Using the correction methods in the exposure tool many of the effects induced by shape and stress can be corrected for if the right algorithms are being used. A detailed analysis of the size of the contributions of material and dimensional tolerances as well as the mask mounting strategy was performed to reach a sample error budget calculation showing the path towards a fulfillment of the ITRS placement requirements for the node studied \(^1\).
1.7. Full Field Mask Development
Due to the upcoming alpha demonstrator EUV exposure tool from ASML, the focus of the mask development has shifted from masks dedicated for micro exposure tool experiments to the needs of a full field mask tool. The printing experiments performed at the MET in Berkeley with absorber binary masks has given valuable insight into the performance and dimensions of the absorber layer stack. This material has been used as a starting point for a full field development. One critical aspect is to achieve the relevant process performance across the size of the quality area (and sometimes even beyond) in the absence of the necessary tools or tool performance. AMTC has developed test mask designs that cover also the outermost regions of the masks and include these into the analysis. Item that were looked at is the blank reflectance performance at the actinic wavelength as well as the optical behavior of all layers in the range between 190 and 1000 nm, the influence of the etch process on these values as well as the more classical items related to the critical dimensions of structures and their placement.

1.8. Inspection and Repair
EUV masks for the 45 nm node and beyond require the detection and subsequent removal of any defect larger than 32 nm. While the detection of defects of this size in patterned masks is not yet possible with the current tool generation, the repair of these defects has been shown to be feasible with e-beam repair techniques. AMTC in 2004 successfully developed a preliminary process for the repair of dark defects based on a nanomachining tool by RAVE. Absorber binary masks with blanks of two different vendors where patterned with programmed defect structures of varying sizes. A detailed study of the edge placement and Z bias behavior and the resulting repair quality was performed. Large structures and structures as small as 20 nm by 100 nm have been successfully removed (Figure 9). The studies included test for over and under repair, i.e. the repair was performed such that the layer underneath was damaged or that the defect was not completely removed before the buffer etch process. It has been demonstrated with wafer prints of these masks at the Berkeley MET tool (Figure 10), that the RAVE tool is capable to repair dark defects on EUV masks. A more detailed analysis of the printing results of the repaired sites is still ongoing and will reveal the limits of the repair technique chosen.

Figure 9 A programmed defect on an absorber binary mask before and after removal with a nanomachining tool.

Figure 10 Resist image of a programmed defect and a corresponding repaired site. The resist image was taken at the MET in Berkeley in cooperation with AMD and Infineon.
1.9. Handling
Special care has to be taken to understand all issues related to the handling of the pellicle-less EUV masks during processing, transport and operations. These aspects are addressed in the EXTUMASK project e.g. concerning the development of a suitable carrier and load lock system for any of the tools involved in the processing of an EUV masks. Within the More Moore project a focus is put on reticle handling starting in the mask house and into the wafer fab and within the exposure tool.

In 2004 Alcatel in close partnership with Incam designed such as carrier and load lock system. They conducted functional and preliminary qualification tests on a first stand alone, vacuum compatible EUV mask carrier/interface prototype. The front end loading port design has been optimized for minimized contamination and for the possible inclusion of additional objects like thermophoresis protection or micro-pumps. The physical realization of the carrier and interface is shown in Figure 11.

The design is capable to accommodate mask holders or frames as being proposed by several parties. Discussions are ongoing with major tool suppliers and potential users of the system for standardization of the system. Figure 11 EUV vacuum capable carrier and load lock system developed by Alcatel and Incam.

Within the More Moore project TNO, ASML and AMTC jointly develop a concept to better understand the issues of mask handling in the wafer fab as depicted in Figure 12. A detailed study of the required handling steps has been conducted to minimize the possibility for contamination and the need for re-cleaning of the masks. A new MEDEA+ project (MUSCLE) started in January 2005 is addressing the harmonization of the supply chain for advanced masks with respect to data flow and material flow. It will certainly be affected by or give valuable input for the choice of a carrier concept for EUV. A fast international agreement on suitable standards in this area is urgently required to focus the development activities of all parties involved.

![Figure 12](image)

Figure 12 Mask handling steps evaluated for possible contamination points

During these activities a new defect classification scheme has been developed. The new scheme accommodates all existing defect types and proposes a consistent nomenclature to incorporate the new defect types that could be present on EUV masks.

3. SUMMARY AND CONCLUSIONS
Companies and public institutes in Europe are actively preparing the path towards a mask production infrastructure for EUV masks for the 45nm node and beyond. The activities in the mask sector are tightly coordinated with the development of the EUV exposure tool in Europe, to allow a timely production of full field masks which will meet the necessary requirements for any given tool generation. The progress over the last three years has been substantial but there is still a long way to go before stable production conditions are reached and the blank material fulfills all requirements. Defect detection sensitivity is still far from sufficient to allow a fast enough development of deposition processes to resolve the key issue of EUV mask making of multilayer defects. Here the joint effort of the worldwide EUV community is required and underway. Likewise the handling of EUV masks along the supply chain and during usage in the wafer fab needs to follow standardized paths to streamline the efforts for building the necessary hardware.

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REFERENCES

5. V. Farys, C. Charpin-Nicole, M. Richard, S. Postnikov, P. Schiavone, J.Y. Robic, E. Quesnel, Investigation of the printability of defects in EUVL mask blank. 3rd International EUV Symposium, Miyazaki, Japan, 2004
8. A. Pawloski et. al., Comparative Study of Mask Architectures for EUV Lithography, Proceedings BACUS 2004